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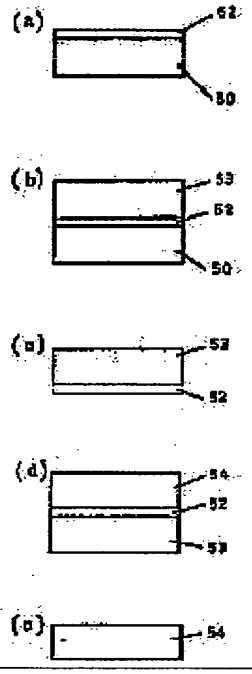
(54) SEMICONDUCTOR SUBSTRATE, MANUFACTURE THEREOF AND SEMICONDUCTOR LIGHT EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a large-area and high-quality industrially practicable GaN semiconductor substrate, a manufacturing method thereof and a semiconductor light emitting element.
SOLUTION: An InrAlsGa1-r-sN ($0 \leq r \leq 1$, $0 \leq s \leq 1$, $r+s \leq 1$) single-crystal film 52 is formed on a first substrate 50, pasted on a second substrate 53 having approximately the same thermal expansion coefficient as that of the InrAlsGa1-r-sN ($0 \leq r \leq 1$, $0 \leq s \leq 1$, $r+s \leq 1$) single crystal and separated from the first substrate 50, an InxAlyGa1-x-yN ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$) single crystal 54 is epitaxially grown on the InrAlsGa1-r-sN single crystal film 52, this film 52 pasted on the second substrate 53, and the InxAlyGa1-x-yN single crystal 54 is separated from the second substrate 53.



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CLAIMS

[Claim(s)]

[Claim 1] The process which forms an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film in the 1st substrate, The process at which an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal and a coefficient of thermal expansion stick an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film on the 2nd almost equivalent substrate, The process which separates an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film from the 1st substrate, On the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film stuck on the 2nd substrate The process which grows epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, According to the proc ss which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrate The production method of the semiconductor substrate characterized by producing an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal as a semiconductor substrate.

[Claim 2] It is the production method of the semiconductor substrate characterized by the 2nd substrate being a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate in the production method of a semiconductor substrate according to claim 1.

[Claim 3] In the production method of a semiconductor substrate according to claim 2 An InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film, The production method of a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate and the semiconductor substrate characterized by all composition of an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal being the same.

[Claim 4] The process which forms an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film in the 1st substrate, The process which separates an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film from th 1st substrate, The process which sticks an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film on the 2nd substrate through a low melting point metal, On the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film stuck on the 2nd substrate, at the temperature beyond the melting point of a low melting point metal The process which grows epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, According to the process which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrate at the temperature beyond the melting point of a low melting point metal The production method of the semiconductor substrate characterized by producing an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal as a semiconductor substrate.

[Claim 5] The process which forms an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film in the 1st substrat , The process which separates an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film from the 1st substrate, The process which sticks an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film on the 2nd substrate through the metal Ga of a melting state, On the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film stuck on the 2nd substrate, at the temperature beyond the melting point of Metal Ga The process made to cool without growing epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, and making Metal Ga solidify, According to th process which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrat at the temp rature beyond the melting point of Metal Ga The production method of the semiconductor substrate characteriz d by producing an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal as a semiconductor substrate.

[Claim 6] It is the production method of the semiconductor substrate characterized by the 1st substrate of the above having th coefficient of thermal expansion of the same grade as an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film in the production method of a semiconductor substrate according to claim 4 or 5.

[Claim 7] The semiconductor substrate characterized by the bird clapper from the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal produced by any 1 term of a claim 1 or a claim 6 by the production method of a publication.

[Claim 8] The semiconductor light emitting device characterized by carrying out the laminating of the GaN system semiconductor laminated structure expressed with general formula InvAlwGa(1-V-W) N (0<=v<=1, 0<=w<=1, v+w<=1) containing at least one PN junction, and constituting it on the semiconductor substrate of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal of a claim 7.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the semiconductor substrate used for the light sources for optical pickups, such as DVD and CD, etc., its production method, and a semiconductor light emitting devic .

[0002]

[Description of the Prior Art] Although brightness is small and blue Light Emitting Diode had a difficulty in utilization conventionally compared with red or green In the GaN system compound semiconductor expressed with a general formula InAlGaN in recent years By having obtained improvement in the crystal-growth technology by using a low-temperature AlN buffer layer or a low-temperature GaN buffer layer, and the p type semiconductor layer of low resistance which doped Mg Blue Light Emitting Diode of high brightness was put in practical use, and further, although it did not result in utilization, th semiconductor laser which carries out continuous oscillation at a room temperature was realized.

[0003] By the way, generally, when growing a quality semiconductor layer epitaxially on a substrate, the lattice constant and coefficient of thermal expansion of a substrate and a semiconductor layer need to be of the same grade. However, at present, the substrate with which a GaN system semiconductor is simultaneously satisfied of these does not exist. Although the attempt which produces a GaN bulk single crystal is made now, the actual condition is that only the about several mm thing is still obtained, and it is in a state far from utilization. Therefore, generally they are sapphire and MgAl 2O4. It is growing up on a substrate which a lattice constant and a coefficient of thermal expansion are large, and is different from a spinel and a GaN system semiconductor like SiC. Therefore, with the GaN system semiconductor, the technology which suppresses generating of the crystal defect which originates in the difference in the lattice constant of a substrate and a semiconductor laser crystal or a coefficient of thermal expansion for production of the semiconductor laser which needs a quality crystal layer is used.

[0004] Drawing 12 is a cross section of the conventional end-face luminescence type semiconductor laser shown in reference "Applied Physics Letters Vol.72(1998) P.211", and although the above technology was used, the number of the semiconductor laser of drawing 12 is also one. The conventional semiconductor laser shown in drawing 12 is formed on the low defective substrate produced combining a selective growth and lateral growth.

[0005] That is, the semiconductor laser of drawing 12 is produced by the following methods. First, the low-temperature buffer layer 112 which consists of n type GaN on the sapphire (2Oaluminum3 single crystal) substrate 111 which makes a principal plane a field (0001) with a thickness of 100-300 micrometers, and the elevated-temperature buffer layer 113 which consists of n type GaN are grown up. Subsequently, SiO2 is deposited on the front face of the n type GaN layer 113, a stripe-like pattern is opened, and the selective-growth mask 114 is formed. Next, the front face of the GaN layer 113 exposed from this mask is made to carry out the selective growth of the GaN. And further, growth is continued, lateral growth of a up to [a mask front face] is performed, finally an n type GaN single crystal layer with a thickness of about 20 micrometers is formed, and it is considering as the substrate for semiconductor laser crystal growths.

[0006] And semiconductor laser structure The n-In0.1Ga0.9N crack prevention layer 115, n-aluminum0.14Ga0.86 N/GaN The MD-SLS (modulation dope strained super lattice) clad layer 116, the n-GaN light-guide layer 117, and In0.15Ga0.85 N/In0.02Ga0.98N The MQW barrier layer 118, the p-aluminum0.2Ga0.8N transposition propagation prevention layer 119, the p-GaN layer light-guide layer 120, the p-aluminum0.14Ga0.86 N/GaNMD-SLS clad layer 121, and the cap layer 122 that consists of a p type GaN layer by the MOCVD method The laminating is carried out one by one. By carrying out dry etching of this semiconductor layer by which the laminating was carried out to the shape of a ridge, an optical waveguide and an optical-resonator end face are formed, and semiconductor laser is formed by forming the n lateral electrode 125 and the p lateral electrode 123 in the cap layer 122 which is a surface of the n-GaN layer 113 exposed by etching, and the semiconductor layer by which the laminating was carried out further, respectively.

[0007] By development of the semiconductor laser formation technology to the low defective substrate top produced combining the selective growth and lateral growth which were shown in drawing 12 , the life of the room temperature continuous oscillation of semiconductor laser is also prolonged with low-power output near the room temperature till about estimated 10000 hours. Concretely, the life of continuous oscillation (20 degrees C and 2mW) is prolonged by such GaN system semiconductor laser of structure till about estimated 10000 hours.

[0008] however, the cleavage plane of the light emitting device which used a conventional GaN system compound semiconductor layer like drawing 12 of a substrate and a GaN system compound semiconductor not necessarily corresponds in order to grow up to be the differ nt-speci s substrate from which the crystal structure differs — ********** — formation of a laser cavity nd fac — laser, such as the conventional AlGaAs system, — it is difficult to carry out by th cleavage method [like]

[0009] In the conv ntional xample of drawing 12 , the optical-r sonator end face is produced by methods, such as dry etching. Therefor , processes, such as removal of formation of the mask for dry etching, dry tching, and a mask, were needed, and the production process was also complicated. Th smooth natur — since it is not yet establish d, there is vertical-reinforcement-like irregularity in th formed r sonator mirror, and the dry tching technology of a GaN system compound semiconductor is formed in th shap of a taper — parallelism, and perpendicularity were not y t still mor enough. Moreover, when a r sonator mirror was formed by dry etching, in order that a substrate might remain as a terrace ahead of a resonator mirror nd fac , light was reflected by this terrace and th shape of beam did not become a single cr st

by it.
[0010] Moreover, since silicon on sapphire was insulation, the light emitting device which used the conventional GaN system compound semiconductor formed on silicon on sapphire was not able to take an l ctrode from a substrate rear face. Ther fore, an lectrode will be formed in an element front fac , and when mounting which forms and carri s out di bonding of the lectrode to a substrate rear face like laser, such as the conventional AlGaAs system, was not able to be performed, the problem that chip area became large only in the part of the space of an electrode also r mained. Moreover, in thermally conductive elevated-temp rature operation from badness or thermally conductive high power operation of silicon on sapphire, the life was extremely short.
[0011] Although the case where a c-th (0001) pag SiC substrate and 2OMgAl(111)4 substrate are used is reported about the GaN system laser element in substrates other than silicon on sapphire, in using a SiC substrate, a crack enters at the time of a crystal growth from the difference in the coefficient of thermal expansion of SiC and a GaN system semiconductor, and formation of the laminated structure of thickness sufficient as laser structure is difficult, and has not resulted in room temperature continuous oscillation. Moreover, (111), since it is insulation like sapphire when using 2OMgAl4 substrate, an electrode cannot be formed in a substrate rear face.
[0012] The report which separated the GaN system semiconductor layer which carried out the crystal growth from the substrate on silicon on sapphire that the trouble of the GaN system semiconductor laser produced by such dissimilar-material substrate should be solved, produced the GaN substrate, and produced GaN system semiconductor laser is also mad .
[0013] Drawing 13 is a cross section of the conventional end-face luminescence type semiconductor laser shown in reference "Jpn.J.Appl.Phys.Vol.37(1998) pp.L309-L312", and the laser structure of the structure as drawing 12 where the semiconductor laser of drawing 13 is the same is formed on a GaN substrate.
[0014] The semiconductor laser of drawing 13 a field (0001) namely, on the substrate 131 with a thickness of 80 micrometers it is thin from GaN made into a principal plane The elevated-temperature buffer layer 132 and the n-In0.1Ga0.9N crack prevention layer 133 which consist of n type GaN, n-aluminum0.14Ga0.86 N/GaN The MD-SLS (modulation dope strained super lattice) clad layer 134, the n-GaN light-guide layer 135, In0.15Ga0.85 N/In0.02Ga0.98N The MQW barrier layer 136, the p-aluminum0.2Ga0.8N transposition propagation prevention layer 137, the p-GaN layer light-guide layer 138, p-aluminum0.14Ga0.86 N/GaN The MD-SLS clad layer 139 and the cap layer 140 which consists of a p type GaN layer by the MOCVD method The laminating is carried out one by one. By carrying out dry etching of this semiconductor layer by which th laminating was carried out to the shape of a ridge, an optical waveguide is formed and semiconductor laser is formed by forming the n lateral electrode 143 and the p lateral electrode 141 in the cap layer 140 which is a surface of the n-GaN layer 132 xposed by etching, and the semiconductor layer by which the laminating was carried out further, respectively. The resonator mirror of laser is produced by the cleavage.
[0015] Thus, on the low defective substrate of the semiconductor laser shown in drawing 12 , the GaN substrate of drawing 13 produces what grew the GaN layer about 100 micrometers instead of the laminated structures 115-122 of semiconductor laser, after that, carries out polish removal of the silicon on sapphire, and is produced as a GaN substrate with a thickn ss of 80 micrometers.
[0016] Moreover, since the end-face luminescence type semiconductor laser shown in drawing 13 is formed on the GaN substrate, formation of a resonator mirror can be performed by the cleavage. Consequently, there was no reflection by th substrate and the shape of beam became a single crest. Moreover, since thermal conductivity is high compared with silicon on sapphire, the thermolysis property improved, high power operation was attained, and, as for the life, 50 degrees C and 30mW operation have also been prolonged till 250 hours.
[0017] Like the example of drawing 13 , after growing up a GaN system semiconductor thickly on a single crystal substrat , a GaN system semiconductor layer is separated from a substrate, and some methods of producing a GaN system semiconductor substrate are proposed. For example, after forming the buffer layer which consists of ZnO on silicon on sapphire and growing up a GaN system semiconductor on it, dissolution removal of the buffer layer is carried out, and the method of separating and producing a substrate and a GaN system semiconductor is indicated by JP,7-202265,A and JP,7-165498,A.
[0018] Moreover, the 1st wafer with which the GaN system semiconductor grew on the 1st substrate, and the 2nd wafer with which the GaN system semiconductor grew on the 2nd substrate are prepared, and as each GaN system semiconductors stick the 1st wafer and 2nd wafer, after pasting up, the method of carrying out polish removal of the 1st substrate and 2nd substrate is indicated by JP,10-229218,A.
[0019]
[Problem(s) to be Solved by the Invention] As mentioned above, by the technology of a low-temperature buffer layer, or the production technology of the low defective substrate by the combination of a selective growth and lateral growth, the crystal growth of the quality GaN system compound semiconductor to a different-species substrates top, such as sapphire, became possible, and reinforcement at the time of low-power output operation near the room temperature of GaN system semiconductor laser was attained. Furthermore, a GaN substrate is produced and an improvement of the property of GaN system semiconductor laser is being expected by using this substrate. However, an industrially utilizable large area and an industrially utilizable quality GaN substrate are not yet realized.
[0020] Since the curvature of a wafer will arise by the production method of the GaN substrate shown in drawing 13 according to the coefficient-of-thermal-expansion difference of GaN and silicon on sapphire if thick GaN is grown up, it is difficult to carry out polish removal of the silicon on sapphire whose diameter is about 2 inches. That is, it was difficult to produce the GaN substrate of a large area by th method of polish removal of a substrate lik before. Moreover, as for the property of semiconductor laser, it was not necessarily good that a def ct was introduced into a GaN layer, crystallinity became bad in process of the silicon-on-sapphir polish for this curvatur , and the thr shold current density of the semiconductor laser produced on it incr ased etc.
[0021] Mor over, as each GaN system semiconductors stick the 1st wafer and 2nd wafer which ar indicated by JP,10-229218,A, after pasting up, sinc a wafer will curv if GaN is thickly grown up by the method of removing the 1st substrat and 2nd substrate, by th differenc in the coefficient of th rmal expansion of a substrat and a GaN system semiconduct r, with the wafer of a large area, GaN syst m semiconductors may not stick complet ly all ov r a waf r. Moreover, a crack may

enter in process of adhesion. Furth rmor , in order to carry out polish removal of the 1st substrat and 2nd substrat , two xpensive substrates will b us d to produc one GaN substrate, and there were also problems, such as b coming high cost.
[0022] Moreover, the technology shown in JP,7-202265,A and JP,7-165498,A, i.e., the technology which produces the GaN substrate which does not r quire polish r moval of a substrate, took the long time very much carrying out dissolution removal of the buffer layer which consists of ZnO of a thin film, and utilization was difficult.
[0023] this invention solves the trouble of the production method of such a conv ntional GaN syst m semiconductor substrate, and aims at offering the semiconductor substrate, its production method, and semiconductor light emitting device of an industrially utilizable large ar a and a quality GaN system.
[0024]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, invention according to claim 1 The process which forms an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film in the 1st substrate, The process at which an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal and a coefficient of thermal expansion stick an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film on the 2nd almost equivalent substrate, The process which separates an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film from the 1st substrate, On the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film stuck on the 2nd substrate The process which grows epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, According to the process which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrate, it is characterized by producing an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal as a semiconductor substrate.
[0025] Moreover, invention according to claim 2 is characterized by the 2nd substrate being a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate in the production method of a semiconductor substrate according to claim 1.
[0026] Moreover, invention according to claim 3 is set to the production method of a semiconductor substrate according to claim 2. An InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film, It is characterized by all composition of a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate and an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal being the same.
[0027] The process at which invention according to claim 4 forms an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film in the 1st substrate, The process which separates an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) singl crystal thin film from the 1st substrate, The process which sticks an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) singl crystal thin film on the 2nd substrate through a low melting point metal, On the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film stuck on the 2nd substrate, at the temperature beyond the melting point of a low melting point metal The process which grows epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, According to the process which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrate at the temperature beyond the melting point of a low melting point metal It is characterized by producing an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal as a semiconductor substrate.
[0028] Moreover, the process at which invention according to claim 5 forms an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film in the 1st substrate, The process which separates an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film from the 1st substrate, The process which sticks an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film on the 2nd substrate through the metal Ga of a melting state, On the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film stuck on the 2nd substrate, at the temperature beyond the melting point of Metal Ga The process made to cool without growing epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, and making Metal Ga solidify, According to the process which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrate at the temperature beyond the melting point of Metal Ga It is characterized by producing an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal as a semiconductor substrate.
[0029] Moreover, as for the 1st substrate of the above, invention according to claim 6 is characterized by having the coefficient of thermal expansion of the same grade as an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film in the production method of a semiconductor substrate according to claim 4 or 5.
[0030] Moreover, invention according to claim 7 is characterized by the bird clapper from the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal with which the semiconductor substrate was produced by any 1 term of a claim 1 or a claim 6 by the production method of a publication.
[0031] A semiconductor light emitting device invention according to claim 8 moreover, on the semiconductor substrate of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal of a claim 7 It is characterized by carrying out the laminating of th GaN system semiconductor laminated structure expressed with general formula InvAlwGa(1-V-W) N (0<=v<=1, 0<=w<=1, v+w<=1) containing at least one PN junction, and constituting it.
[0032]
[Embodiments of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing. Drawing 1 is drawing showing the example of a production process of the semiconductor substrate concerning this invention. The process which forms the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 in the a. 1st substrate 50 (single crystal substrate) in the example of a production process of drawing 1 (drawing 1 (a)), b. The process at which an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal and a coefficient of thermal expansion stick the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 on the 2nd almost equivalent substrate 53 (drawing 1 (b)), c. Th process which separates the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 from the 1st substrat (single crystal substrate) 50 (drawing 1 (c)), d. on the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 stuck on the 2nd substrat 53 The proc ss which grows pitaxially the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 (drawing 1 (d)), . It has the proc ss (drawing 1 ( )) which separates the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 from the 2nd substrate 53. Finally, th InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrat 54 is produced.
[0033] Her , as the 1st substrat (single crystal substrat) 50, the c-th page (0001) of sapphire, the a-th page (11-20) of sapphire, MaAl2O4 spin l (111) sides, th c-th page (0001) of 6 H-SiC, the m-th page (1-100) of 6 H-SiC etc., etc. are usable.
[0034] Moreov r, in the process of a, as the crystal-growth method of the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52, although meanses, such as MOCVD, HVPE, and MBE, are usabl Y u may use the other m thods,

as long as it is the method that the crystal growth of the InrAlsGa(1−r−s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 can be carried out to the 1st substrate (single crystal substrate) 50 inst ad of what is limited to the abov −mentioned method. Moreover, in case the InrAlsGa(1−r−s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 is grown up The surface layer of th crystal layer which did not interfere even if it deposited low−temperature buffer layers, such as GaN and AlN, previously, and grew using the 1st substrate (single crystal substrate) 10 should just be an InrAlsGa(1−r−s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal.

[0035] In the process of b as th 2nd substrate 53 Mor over, a single crystal Or the molybdenum substrate (6x10−6k−1) of a polycrystal, single crystal YAlO3 substrate, a single crystal GGG (Gd3Ga 5O12) substrate, Or the single crystal which adjusted raw material composition and was produced so that a coefficient of th rmal xpansion might becom of the sam grade as the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54, polycrystal, or an amorphous object is usable.

[0036] moreover, as a method of sticking on the 2nd substrate 53 Although it is possible to heat a wafer in the nitrogen−gas−atmosphere mind pressurized more than the decomposition pressure of a nitride semiconductor, and to paste up the InrAlsGa (1−r−s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 and the 2nd substrate 53 directly by diffused junction If it is th method which does not have trouble in growing epitaxially the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 in removal of the 1st substrate 50 in the process of c, and the process of d, it will not interfere, even if it is the other methods.

[0037] The grade of attachment moreover, the whole surface surface of the InrAlsGa(1−r−s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 If it is the grade which does not have trouble in it not being completely joined to the 2nd substrat 53, and growing epitaxially the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 in removal of the 1st substrate 50 in the process of c, or the process of d It does not interfere by the grade joined partially, either. Moreover, the bonding strength does not have trouble in growing epitaxially the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 in removal of the 1st substrate 50 in the process of c, or the process of d, and even if weak, it does not interfere.

[0038] Moreover, in the process of c, as a method of separating the 1st substrate (single crystal substrate) 50 from the InrAlsGa(1−r−s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52, although chemical etching, polish, etc. are usable, it is not limited especially and is usable suitably.

[0039] In the process of d, moreover, on the InrAlsGa(1−r−s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film 52 stuck on the 2nd substrate 53 As a method of growing epitaxially, the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 Although not limited especially, since a thick single crystal layer is grown up, the quick method of growth rates, such as th HVPE method and the high−speed MOCVD method, is desirable. Moreover, it is possible by doping n type and p type dopant to control a conduction type.

[0040] Moreover, in the process of e, as a method of separating the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 from the 2nd substrate 53, although chemical etching, polish, etc. are usable, it is not limited especially and is possible suitably.

[0041] Drawing 2 is drawing showing the example of the example of a production process shown in drawing 1 . In the example of a process of drawing 2 , the n type GaN single crystal substrate is produced as a semiconductor substrate.

[0042] If drawing 2 is referred to, first, ammonium will be used for an III group raw material by making hydrogen gas into carrier gas at 520 degrees C at trimethylgallium and V group raw material, about 25nm of GaN buffer layers 51 will be deposited on c−th (0001) page silicon on sapphire 50 with a diameter of 2 inches, a temperature up will be carried out to 1050 degrees C after that, and 8 micrometers will grow the GaN single crystal layer 52 (drawing 2 (a)).

[0043] Subsequently, the polycrystal Mo substrate 53 which carried out polishing of the front face and was made into th shape of a mirror plane, and the front face of the GaN single crystal 52 are stuck, and it transports to an annealer in the state where it fixed strongly with the heat−resistant fixture. And in 20 in nitrogen−gas−atmosphere mind atmospheric pressure, and 1100 degrees C, annealing is performed and diffused junction of both is carried out (drawing 2 (b)).

[0044] Subsequently, polish equipment is used and polish removal of the sapphire (0001) substrate 50 is carried out (drawing 2 (c)). At this time, since the GaN buffer layer 51 is a layer containing the polycrystal layer which grew at low temperature, it carries out polish removal simultaneously, and it carries out polishing of the front face of the exposed GaN single crystal layer 52 to the shape of a mirror plane further.

[0045] Subsequently, the Mo substrate 53 is transported to HVPE equipment, by making N2 gas into carrier gas, in a metal gallium and V group raw material, a silicon tetrachloride (SiCl4) is used for HCl gas and an III group raw material, and 300 micrometers grows up [in a raw material] the n type GaN single crystal 54 to be reactant gas at ammonia gas and n type dopant gas at the front face of the GaN single crystal layer 52 exposed at 1050 degrees C (drawing 2 (d)).

[0046] Subsequently, polish equipment is used and polish removal of the Mo substrate 53 is carried out. Furthermore, polishing of the front face of the exposed GaN single crystal layer 54 is carried out to the shape of a mirror plane, and th n type GaN single crystal substrate 54 with a thickness of 300 micrometers is produced (drawing 2 (e)). Thus, an n type GaN single crystal substrate is producible as a semiconductor substrate.

[0047] In drawing 1 and the example of a production process of drawing 2 , by taking an above−mentioned process, there are no generating and curvature of a crack by growing up to be the big substrate 50 of a coefficient−of−thermal−expansion difference thickly, and the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 54 of a practical area is produced. Moreover, since the crystal structure or lattice constant will not interfere even if they differ from each other if the 2nd substrate 53 has the coefficient of thermal expansion almost equivalent to the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 The width of face of substrate selection increases and the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrat 54 is produced by th low cost by choosing a cheap substrat .

[0048] By the way, by above−mentioned drawing 1 and the production method of drawing 2 , when th 2nd substrate 53 which consists of a different material from th InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) singl crystal 54 was used, there was a case where restrictions were attached to crystal−growth conditions, such as crystal−growth temperature and growth atmospher , by the 2nd melting point and chemical stability of a substrat . Moreover, th concern diffused as an impurity into the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 also had the composition element of the 2nd substrat 53.

[0049] In order t avoid such a probl m, it is good t use the 2nd substrate 53 as th polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate which consists of an InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer

54 and a material of the same kind. That is, it is good to use the 2nd substrate 53 as a polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate.

[0050] Drawing 3 is drawing showing the example of a production process in the case of using the 2nd substrate 53 as a polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate. In addition, in the xample of drawing 3 , the n type In0.1Ga0.9N single crystal substrat is produced as a semiconductor substrate.

[0051] If drawing 3 is referred to, first, ammonium will be used for an III group raw material by making hydrog n gas into carrier gas at 520 degrees C at trimethylgallium and V group raw mat rial, about 25nm of GaN buffer layers 51 will be deposited on c−th (0001) page silicon on sapphir 50 with a diam ter of 2 inches, a temperatur up will be carried out to 1050 degr es C after that, and 8 micrometers will grow the GaN single crystal layer 52 (drawing 3 (a)).

[0052] Subsequently, the front face of the polycrystal GaN substrate 53 which carried out polishing of the front face and was made into the shape of a mirror plane, and the GaN single crystal layer 52 is stuck (drawing 3 (b)), and it transports to an annealer in the state where it fixed strongly with the heat−resistant fixture. And in 20 in nitrogen−gas−atmosphere mind atmospheric pressure, and 1100 degrees C, annealing is performed and diffused junction of both is carried out.

[0053] Subsequently, polish equipment is used and polish removal of the sapphire (0001) substrate 50 is carried out. At this time, since the GaN buffer layer 51 is a layer containing the polycrystal layer which grew at low temperature, it carries out polish removal simultaneously, and it carries out polishing of the front face of the exposed GaN single crystal layer 52 to the shap of a mirror plane further (drawing 3 (c)).

[0054] Subsequently, the polycrystal GaN substrate 53 is transported to MOVPE equipment, a mono silane is used for an III group raw material in ammonia gas, a monomethylhydrazine, and n type dopant gas by making N2 gas into carrier gas at trimethylgallium, trimethylindium, and V group raw material, and 200 micrometers grows up the n type In0.1Ga0.9N singl crystal 54 to be the front face of the GaN single crystal layer 52 exposed at 800 degrees C (drawing 3 (d)).

[0055] Subsequently, polish equipment is used and polish removal of the polycrystal GaN substrate 53 is carried out. Furthermore, polishing of the front face of the exposed GaN single crystal layer 54 is carried out to the shape of a mirror plane, and the n type In0.1Ga0.9N single crystal substrate 54 with a thickness of about 200 micrometers is produced (drawing 3 (e)).

[0056] Thus, since the 2nd substrate 53 is a polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate according to the xample of a process of drawing 3 There are no generating and curvature of a crack by growing up to be the big substrate of a coefficient−of−thermal−expansion difference thickly, and the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 54 of a practical area is produced. Moreover, since the composition element is the same, mixing of the impurity from a substrate is reduced.

[0057] by the way, in the example of a production process of drawing 3 By using the polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate which turns into the 2nd substrate 53 from the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 54 and a material of the same kind Although the concern which loses the restrictions by the 2nd substrate 53 of the growth conditions of the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 54, and the composition element of a substrate 53 mixes as an impurity was reduced The polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate 53 Since mixed−crystal composition differs, a coefficient of thermal expansion differs from an InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer in the 2nd substrate 53 and the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 54. Therefore, we are anxious about a defect occurring for the heat distortion resulting from a coefficient−of−thermal−expansion difference.

[0058] In order to avoid such a problem, it sets for the example of a production process of drawing 3 . InrAlsGa N (1−r−s) (0<=r<=1, 0<=s<=1, r+s<=1) Composition of the single crystal thin film 52, the polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate 53, and the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 It is good to make all the same, to make mostly the coefficient−of−thermal−expansion difference of the 2nd substrate 53 and the crystal layer 54 into z ro, and to reduce generating of the defect by heat distortion.

[0059] Drawing 4 InrAlsGa N (1−r−s) (0<=r<=1, 0<=s<=1, r+s<=1) Composition of the single crystal thin film 52, the polycrystal IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate 53, and the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 It is drawing showing the example of a production process in the case of making all the same. In addition, in th xample of drawing 4 , the n type aluminum0.15Ga0.85N single crystal substrate is produced as a semiconductor substrate.

[0060] If drawing 4 is referred to, first, ammonium will be used for an III group raw material by making hydrogen gas into carrier gas at 520 degrees C at trimethylgallium and V group raw material, about 25nm of aluminum0.15Ga0.85N buffer layers 51 will be deposited on c−th (0001) page silicon on sapphire 50 with a diameter of 2 inches, a temperature up will be carri d out to 1050 degrees C after that, and 8 micrometers will grow the aluminum0.15Ga0.85N single crystal layer 52 (drawing 4 (a)).

[0061] Subsequently, the polycrystal aluminum0.15Ga0.85N substrate 53 which carried out polishing of the front face and was made into the shape of a mirror plane, and the front face of the aluminum0.15Ga0.85N single crystal 52 are stuck (drawing 4 (b)), and it transports to an annealer in the state where it fixed strongly with the heat−resistant fixture. And in 20 in nitrogen−gas−atmosphere mind atmospheric pressure, and 1100 degrees C, annealing is performed and diffused junction of both is carried out.

[0062] Subsequently, polish equipment is used and polish removal of the sapphire (0001) substrate 50 is carried out. At this time, since the aluminum0.15Ga0.85N buffer layer 51 is a layer containing the polycrystal layer which grew at low t mperature, it carries out polish removal simultan ously, and it carries out polishing of the front face of the exposed aluminum0.15Ga0.85N single crystal layer 52 to the shape of a mirror plan further (drawing 4 (c)).

[0063] Subsequently, the aluminum0.15Ga0.85N substrat 53 is transported to MOVPE quipment, a mono silane is used for an III group raw material in ammonia gas and n type dopant gas by making H2 gas into carrier gas at trimethylgallium, a trimethylaluminum, and V group raw material, and 300 micrometers grows up the n type aluminum0.15Ga0.85N single crystal 54 to be th front fac of the aluminum0.15Ga0.85N singl crystal layer 52 exposed at 1050 degr es C (drawing 4 (d)).

[0064] Subsequently, polish equipment is used and polish removal of the polycrystal aluminum0.15Ga0.85N substrate 53 is carried out. Furthermore, polishing of th front face of the exposed aluminum0.15Ga0.85N singl crystal layer 54 is carried out to the shap of a mirror plane, and the n typ aluminum0.15Ga0.85N single crystal substrate 54 with a thickn ss of 300 micrometers is produced (drawing 4 ( )).

[0065] Although the above-mentioned example showed th xample which produc s an n type aluminum0.15Ga0.85N single crystal substrat as a s miconductor substrate, an n type GaN single crystal substrate is also producible as other examples. Drawing 4 which m ntioned above the method of producing an n type GaN single crystal substrate for convenienc is us d and explained.

[0066] As a semiconductor substrate, when producing an n typ GaN single crystal substrate, first, ammonium is used for an III group raw material by making hydrogen gas into carri r gas at 520 degrees C at trimethylgallium and V group raw material, about 25nm of GaN buffer layers 51 is deposited on c-th (0001) page silicon on sapphir 50 with a diam ter of 2 inches, a temperature up is carried out to 1050 degrees C after that, and 8 micrometers grows the GaN single crystal layer 52 (drawing 4 (a)).

[0067] Subsequently, the polycrystal GaN substrate 33 and the front face of the GaN single crystal 32 are stuck (drawing 4 (b)), and it transports to an annealer in the state where it fixed strongly with the heat-resistant fixture. And in 20 in nitrogen-gas-atmosphere mind atmospheric pressure, and 1100 degrees C, annealing is performed and diffused junction of both is carried out.

[0068] Subsequently, polish equipment is used and polish removal of the sapphire (0001) substrate 50 is carried out. At this time, since the GaN buffer layer 51 is a layer containing the polycrystal layer which grew at low temperature, it carries out polish removal simultaneously, and it carries out polishing of the front face of the exposed GaN single crystal layer 52 to the shape of a mirror plane further (drawing 4 (c)).

[0069] Subsequently, the polycrystal GaN substrate 53 is transported to HVPE equipment, by making N2 gas into carrier gas, in a metal gallium and V group raw material, a silicon tetrachloride (SiCl4) is used for HCl gas and an III group raw material, and 300 micrometers grows up [in a raw material] the n type GaN single crystal 54 to be reactant gas at ammonia gas and n type dopant gas at the front face of the GaN single crystal layer 52 exposed at 1050 degrees C (drawing 4 (d)).

[0070] Subsequently, polish equipment is used and polish removal of the polycrystal GaN substrate 53 is carried out. Furthermore, polishing of the front face of the exposed GaN single crystal layer 54 is carried out to the shape of a mirror plane, and the n type GaN single crystal substrate 54 with a thickness of 300 micrometers is produced (drawing 4 (e)).

[0071] Thus, according to the example of a production process of drawing 4 InrAlsGa N (1-r-s) The single crystal thin film 52, (0<=r<=1, 0<=s<=1, r+s<=1) Since all composition of the polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate 53 and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54 is the same Rather than the production method of drawing 3 , generating and the curvature of a crack by the coefficient-of-thermal-expansion difference are reduced further, and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 54 of a practical area still more nearly quality than the production method of drawing 3 is produced. Moreover, since the composition element is the same, the impurity from a substrate is also reduced.

[0072] In this invention, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 54 produced by each production method which was mentioned above can be offered. And the conductive substrate which shows a desired conduction type can be offered by doping n type and p type dopant at the process which grows the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 54.

[0073] That is, in this invention, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate of the large area which a GaN system semiconductor and a coefficient-of-thermal-expansion difference are not almost, and was equipped with grid adjustment, thermal conductivity, cleavage, and conductivity can be offered. Moreover, since the c-th page (0001) of sapphire, the a-th page (11-20) of sapphire, MgAl2O4 spinel (111) sides, the c-th page (0001) of 6 H-SiC, the m-th pag (1-100) of 6 H-SiC etc., etc. are usable, the 1st substrate 50 By the direction of a field of a substrate, it becomes the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate which makes a principal plane the c-th (0001) pag and the m-th (1-100) page. For example, if the c-th page (0001) of sapphire, the a-th page (11-20) of sapphire, MgAl2O4 spinel (111) sides, and the c-th page (0001) of 6 H-SiC are used for the 1st substrate 50 (0001) If it becomes the InxAlyGa (1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate which makes the c-th page a principal plane and the m-th page (1-100) substrate of 6 H-SiC is used (1-100) It becomes the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate which makes the m-th page a principal plane.

[0074] Moreover, on the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 54 produced in this invention as mentioned above The laminating of the GaN system semiconductor laminated structure expressed with general formula InvAlwGa(1-V-W) N (0<=v<=1, 0<=w<=1, v+w<=1) containing at least one PN junction is carried out, and a semiconductor light emitting device can be offered.

[0075] Current is impressed to the electrode corresponding to p type of a semiconductor light emitting device, and n type lay r, current is poured into PN junction, and a semiconductor light emitting device emits light by the reunion of a carrier. It has at least one PN junction, and current is poured into this PN junction, and if the GaN system compound semiconductor laminated structure which constitutes a semiconductor light emitting device is structure which emits light by the reunion of a carrier, no matter they may be homozygous, a single heterojunction, a double heterojunction, quantum well structure, multiplex quantum well structure, and what other structures, it will not interfere.

[0076] Moreover, in this invention, since the cleavage was possible for the substrate, when the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 54 was used for the substrate of a semiconductor light emitting device, and a semiconductor light emitting device is made into semiconductor laser, it can have a laser resonator mirror by the good cleavage of parallelism and smooth nature. Furthermore, it is possible by making a substrate into conductivity to consider as th light emitting device which had th el ctrode formed in a substrate rear face (namely, thing for which n type and p type dopant are doped to the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 54).

[0077] Drawing 5 is drawing showing the example of the semiconductor light emitting device concerning this invention. In addition, the semiconductor light emitting device of drawing 5 is constituted as semiconductor laser. If drawing 5 is r ferred to, this semiconductor light emitting device on the n-aluminum0.15Ga0.85N single crystal substrate 54 produced by the production method which was mentioned abov The n-GaN buffer layer 31, the n-aluminum0.15Ga0.85N clad layer 32, the n-GaN light-guide layer 33, the In0.15Ga0.85 N/In0.02Ga0.98N multiplex quantum well structur barrier layer 34, the p-GaN light-guide layer 35, It has the laminat d structure to which the laminating of the p-aluminum0.15Ga0.85N clad layer 36 and the p-GaN cap layer 37 was carried out one by one.

[0078] And th ridge structure where ********** using a remnants strike rye pattern with a width of fac of 5 micromet rs,

and from the front fac of th p type GaN cap layer 37 of this laminated structure to th middl of th p-aluminum0.15Ga0.85N clad layer 36 serv s as a waveguide is formed. Here, the dir ction of a waveguide is th <1-100> direction.

[0079] Thus, the protective layer 38 which consists of SiO2 has accumulated on p-aluminum0.15Ga0.85N clad lay r 36 front face expos d by forming ridge structure. Moreover, the p side ohmic electrode 39 is formed on the p-GaN cap lay r 37. Moreov r, the n side ohmic electrod 40 is formed in th rear face of the n-aluminum0.15Ga0.85N singl crystal substrate 54. The optical-resonator side of this semiconductor laser is formed by carrying out the cleavage of the m-th (1-100) page.

[0080] In the semiconductor light mitting device of drawing 5 , the crystal growth of th n-GaN buffer layer 31, the n-aluminum0.15Ga0.85N clad layer 32, the n-GaN light-guide layer 33, the In0.15Ga0.85 N/In0.02Ga0.98N multiplex quantum well structure barrier layer 34, the p-GaN light-guide layer 35, the p-aluminum0.15Ga0.85N clad layer 36, and the p-GaN cap lay r 37 was carried out by the MOCVD method.

[0081] Moreover, the p side ohmic electrode 39 carried out vacuum deposition, and it is 700 degrees C in temperature, and Au/Pt/nickel was heat-treated for 20 minutes and it formed it. Moreover, the n side ohmic electrode 40 carried out vacuum d position of aluminum/Ti, heat-treated it, and formed it.

[0082] If current is impressed to the p side ohmic electrode 39 and the n side ohmic electrode 40, current is poured into the In0.15Ga0.85 N/In0.02Ga0.98N multiplex quantum well structure barrier layer 34, and the semiconductor laser of drawing 5 emits light by the reunion of a carrier, and reflective amplification will be repeated by the resonator side formed of the cleavage, and it will be outputted outside as a laser beam.

[0083] In the semiconductor laser of drawing 5 , the clad layer which a crack could not go into a substrate 54 easily at the time of a crystal growth even if it enlarged the mixed-crystal ratio of aluminum of a clad layer compared with the case where sapphire and a GaN substrate are used, since the n-aluminum0.15Ga0.85N single crystal substrate of the same composition as a clad layer was used, therefore equipped it with sufficient composition and sufficient thickness of light to shut up can be formed. Consequently, there is no aggravation of the shape of beam by the leakage of the light from a clad layer, and semiconductor laser with low oscillation threshold current density is produced.

[0084] Drawing 6 is drawing showing other examples of a production process of the semiconductor substrate concerning this invention. The process which forms the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 in the a. 1st substrate 10 (single crystal substrate) in the example of a production process of drawing 6 (drawing 6 (a)), b. The process which separates the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 from the 1st substrate (single crystal substrate) 10 (drawing 6 (b)), c. The process which sticks the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 on the 2nd substrate 15 through the low melting point metal 16 (drawing 6 (c)), d. On the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 stuck on the 2nd substrate 15, at the temperature beyond the melting point of the low melting point metal 16 The process which grows epitaxially the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 (drawing 6 (d)), e. It has the process (drawing 6 (e)) which separates the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 from the 2nd substrate 15 at the temperature beyond the melting point of th low melting point metal 16. Finally, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17 is produced.

[0085] Here, as the 1st substrate (single crystal substrate) 10, the c-th page (0001) of sapphire, the a-th page (11-20) of sapphire, MaAl2O4 spinel (111) sides, the c-th page (0001) of 6 H-SiC, the m-th page (1-100) of 6 H-SiC etc., etc. are usable.

[0086] Moreover, in the process of a, as the crystal-growth method of the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) singl crystal thin film 12, although MOCVD, HVPE, MBE, etc. are usable You may use the other methods, as long as it is th method that the crystal growth of the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 can be carried out to the 1st substrate (single crystal substrate) 10 instead of what is limited to the above-mentioned method. Moreov r, before growing up the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 The surface layer of the crystal layer which did not interfere even if it deposited previously low-temperature buffer layers, such as GaN and AlN, and other layers, and grew using the 1st substrate (single crystal substrate) 10 should just be an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal.

[0087] moreover, in the process of b, as a method of separating the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) singl crystal thin film 12 from the 1st substrate (single crystal substrate) 10 After sticking the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 on a support substrate, The method of removing the 1st substrate (single crystal substrate) 10 by methods, such as chemical etching and polish Between the 1st substrate (single crystal substrate) 10 and the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal layer 12 Although the way ********** the layer and a lift off separates the 1st substrate (single crystal substrate) 10 etc. is usable after growing up the layer which can be etched, it is not limited to the above-mentioned method, especially concerning the method of separation.

[0088] Moreover, in the process of c, as long as the melting point is a low thing as a low melting point metal 16 from th growth temperature of InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1), and the temperature which separates the 2nd substrate 15, a single metal or an alloy is sufficient. For example, an indium, tin, a gallium, etc. are usable. Moreover, if stable [in the growth temperature and growth atmosphere] as the 2nd substrate 15 in case an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal is grown epitaxially at a next process, it is good, and a single crystal, polycrystal, and an amorphous substance are not asked for sapphire, Si, a quartz, etc., but it is usable.

[0089] In the process of d, on the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 stuck on the 2nd substrat 15, moreover, at the temperature beyond th melting point of the low m lting point metal 16 When growing epitaxially th InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17, The IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 Since it is on molten metal 16, the crystal growth of a singl crystal 17 progress s without being influenced of the coefficient-of-thermal-expansion difference of the 2nd substrate 15 and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) singl crystal 17, the difference in the crystal structur , etc. Although it does not limit, since specially the method of a crystal growth grows the thick single crystal layer 17, its quick method f growth rates, such as th HVPE method and the high-sp ed MOCVD method, is desirabl . Moreover, it is possibl by doping n type and p typ dopant to control a conduction type.

[0090] Drawing 7 and drawing 8 are drawings showing the example of the example of a production proc ss shown in drawing

6 . In drawing 7 and the example of a process of drawing 8 , th n typ GaN single crystal substrate is produced as a semiconductor substrate.
[0091] If drawing 7 and drawing 8 are referred to, the GaN layer 12 will be first grown up by the MOCVD method on c-th (0001) page silicon on sapphire 10 with a diameter of 2 inches. Growth of the GaN layer 12 is performed by the MOCVD method, ammonia is us d for an III group raw material by making hydrogen gas into carrier gas at 520 d gr es C at trimethylgallium and V group raw material, about 25nm of GaN buffer layers 11 is deposited, and a temperatur up is carried out to 1050 degrees C after that, and it is made when 10 micrometers grows the GaN single crystal layer 12 (drawing 7 (a)).
[0092] Subsequently, the front face of the GaN single crystal layer 12 is pasted up on the support substrat 14 with the adhesives 13 of an organic system (drawing 7 (b-1)), and, subsequently polish removal of the silicon on sapphire 10 is carried out with polish equipment (drawing 7 (b-2)).
[0093] Subsequently, the quartz substrate 15 and the GaN single crystal layer 12 are pasted up by the indium 16 (drawing 7 (c-1)). Here, an indium 16 is carried on the quartz substrate 15, as the adhesion method, further, GaN single crystal layer 12 front face is made into an indium 16 side, and is carried, and the GaN single crystal layer 12 stuck on the support substrat 14 on it is heated to the temperature beyond the melting point of an indium 16, and an indium 16 is changed into a melting state and it pastes up.
[0094] After an appropriate time, the adhesives 13 of an organic system are dissolved by the organic solvent, and the support substrate 14 is separated (drawing 8 (c-2)).
[0095] Subsequently, transport the quartz substrate 15 which pasted up the GaN single crystal layer 12 to HVPE equipment, and N2 gas is made into carrier gas. Moreover, a silicon tetrachloride (SiCl4) is used for HCl gas and an III group raw material, and the n type GaN single crystal 17 is grown up [in a raw material / at a metal gallium and V group raw material] to b reactant gas in the thickness of 300 micrometers at 1050 degrees C in ammonia gas and n type dopant gas at the front face of the GaN single crystal layer 12 (drawing 8 (d)).
[0096] Subsequently, the quartz substrate 15 which grew the n type GaN single crystal layer 17 is heated to the temperatur beyond the melting point of an indium 16, an indium 16 is changed into a melting state, and the quartz substrate 15 is separated (drawing 8 (e-1)). After an appropriate time, polish equipment is used, polish removal of the GaN buffer layer 11 is carried out, further, polishing of the front face of the GaN single crystal layer 17 is carried out to the shape of a mirror plane, and the n type GaN single crystal substrate 17 with a thickness of about 300 micrometers is produced (drawing 8 (e-2)). Thus, an n type GaN single crystal substrate is producible as a semiconductor substrate.
[0097] In drawing 6 , drawing 7 , and the example of a production process of drawing 8 , by the cooling process after the crystal growth of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 Since the congealing point of the low melting point metal 16 has not combined the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 with a substrate 15 The InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 as for a thing of a large area Generating and the curvature of a crack by the thermal-contraction difference of the substrate 15 and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 at the time of cooling from crystal-growth temperature to the congealing point of the low melting point metal 16 are reduced. Therefore, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17 of the large area by which a crack and curvature were reduced is producible.
[0098] Moreover, since separation of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 from th 2nd substrate 15 can be performed easily and can be reused, without damaging the 2nd substrate 15, low-cost-ization is attained. Furthermore, since a single crystal, polycrystal, an amorphous substance, etc. can be used for the 2nd substrate 15, low-cost-ization is attained by the width of face of substrate selection spreading and choosing a cheap substrate.
[0099] In addition, Ga (gallium) which has the melting point near the room temperature (about 30 degrees C) as a low m lting point metal 16 is used at the process (drawing 6 (c)) of c mentioned above. From epitaxial growth of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 in the process (drawing 6 (d), (e)) of d and e to separation of the 2nd substrat 15 can also be performed without making Ga solidify.
[0100] namely, -- this case -- a. -- with the process (drawing 6 (a)) which forms the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 in the 1st single crystal substrate 10 b. The process which separates the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 from the 1st single crystal substrate 10 (drawing 6 (b)), c. The process which sticks the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 on the 2nd substrate 15 through the metal Ga(gallium) 16 of a melting state (drawing 6 (c)), d. On the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 stuck on the 2nd substrate 15, at the temperature beyond the melting point of a metal Ga(gallium) 16 The process made to cool without growing epitaxially the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17, and making a metal Ga(gallium) 16 solidify (drawing 6 (d)), e. It has the process (drawing 6 (e)) which separates the InxAlyGa (1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 from the 2nd substrate 15 at the temperature beyond the melting point of a metal Ga(gallium) 16. Finally, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17 is produced.
[0101] Thus, Ga which has the melting point near the room temperature (about 30 degrees C) as a low melting point metal 16 is used at the process (drawing 6 (c)) of c. From epitaxial growth of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 in the process (drawing 6 (d), (e)) of d and e Because it is made to perform even separation of the 2nd substrate 15, without making Ga solidify It becomes possible to produce a single crystal substrate, without being influenced at all of heat distortion by the cooling process after the crystal growth by the coefficient-of-thermal-expansion difference of the 2nd substrate 15 and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17.
[0102] Ga which has the melting point n ar the room t mperature (about 30 degrees C) as a low melting point metal 16 is used, and the example in the case of performing from pitaxial growth of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 to separation of the 2nd substrate 15, without making Ga solidify is explained. In addition, by this example, the n type GaN singl crystal substrate is pr duc d as a semiconductor substrat .
[0103] By this exampl , the GaN layer 12 is first grown up by MOCVD on c-th (0001) page silicon n sapphire 10 with a diameter of 2 inch s. Growth of the GaN lay r 12 is p rformed by MOCVD, ammonia is used for an III group raw material by making hydrogen gas into carrier gas at 520 degrees C at trimethylgallium and V group raw mat rial, about 25nm of GaN buffer layers 11 is deposit d, and a t mperature up is carried out to 1050 degrees C after that, and it is made wh n 10 micromet rs grows th GaN single crystal layer 12 (drawing 7 (a)).

[0104] Subsequently, the front face of the GaN singl crystal layer 12 is pasted up on the support substrate 14 with th adhesiv s 13 of an organic system (drawing 7 (b-1)), and, subsequ ntly polish removal of the silicon on sapphir 10 is carri d out with polish equipment (drawing 7 (b-2)).
[0105] Subsequently, the quartz substrate 15 and the GaN single crystal layer 12 ar past d up by Ga (gallium)16 (drawing 7 (c-1)). Here, Ga(gallium) 16 is carried on the quartz substrate 15, as the adhesion method, further, GaN single crystal lay r 12 front face is made into Ga(gallium) 16 side, and is carried, and th GaN single crystal layer 12 stuck on th support substrate 14 on it is heated to the temp rature beyond the melting point of Ga (gallium)16, and Ga (gallium)16 is changed into a melting state, and it pastes up.
[0106] After an appropriat time, the binder 13 of an organic syst m is dissolv d by the organic solv nt, and th support substrate 14 is separated (drawing 8 (c-2)). Temperature at this time is made below into the melting point of Ga(gallium) 16.
[0107] Subsequently, transport the quartz substrate 15 which pasted up the GaN single crystal layer 12 to HVPE equipment, and N2 gas is made into carrier gas. Moreover, a silicon tetrachloride (SiCl4) is used for ammonia gas and n type dopant gas to reactant gas in a metal gallium and V group raw material at HCl gas and an III group raw material. The n type GaN single crystal 17 is grown up to be the thickness of 300 micrometers on the front face of the GaN single crystal substrate 12 at 1050 d grees C (drawing 8 (d)).
[0108] Subsequently, it cools to 35 degrees C beyond the melting point of Ga(gallium) 16 after growth of the n type GaN single crystal 17, this temperature is held, and the quartz substrate 15 is separated (drawing 8 (e-1)). After an appropriat time, polish equipment is used, polish removal of the GaN buffer layer 11 is carried out, further, polishing of the front fac of the GaN single crystal layer 17 is carried out to the shape of a mirror plane, and the n type GaN single crystal substrate 17 with a thickness of about 300 micrometers is produced (drawing 8 (e-2)). Thus, an n type GaN single crystal substrate is producible as a semiconductor substrate.
[0109] Thus, Ga which has the melting point near the room temperature (about 30 degrees C) as a low melting point metal 16 is used at the process (drawing 6 (c)) of above-mentioned c. From epitaxial growth of the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17 in the process (drawing 6 (d), (e)) of d and e to separation of the 2nd substrate 15 can also be performed without making Ga solidify. In this case, also in the cooling process in the crystal growth of the InxAlyGa (1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17, and after growth, since a metal Ga(gallium) 16 is in a melting state The InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 is not combined with the 2nd substrate 15. Therefore, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 Also at the time of cooling after a growth end, since the inside of a crystal growth is not influenced at all of the heat distortion by the coefficient-of-thermal-expansion difference of the 2nd substrate 15 and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17, either Even if it makes the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 into a large area, ther are no generating and curvature of a crack. Therefore. the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrat 17 of the large area by which a crack and curvature were reduced is producible.
[0110] Moreover, since a single crystal, polycrystal, an amorphous substance, etc. can be used for the 2nd substrate 15, the width of face of substrate selection spreads and it can choose a cheap substrate. Furthermore, since the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 can be easily separated from the 2nd substrate 15, without damaging the 2nd substrate 15, reuse of a substrate is possible. Therefore, low-cost-ization is attained. Moreover, since the same Ga as a base material element is used for a low melting point metal, the impurity contamination by the low melting point metal is r duced.
[0111] Moreover, as for the 1st substrate (single crystal substrate) 10, in the example of a production process mentioned above, it is good to have the coefficient of thermal expansion of the same grade as the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12.
[0112] Namely, on it, the 1st substrate (single crystal substrate) 10 has the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 and coefficient of thermal expansion of the same grade which carry out a crystal growth, and the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 should just carry out a crystal growth. For example, in GaN, GaAs, GGG (Gd3Ga 5O12), etc. can be used. using GaAs (100) in GaAs -- a cubic -- hexagonal by GaN growing and using GaAs (111) -- GaN can be grown up
[0113] Thus, the 1st substrate (single crystal substrate) 10 By having the coefficient of thermal expansion of the same grade as th IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 The curvature and crack which are generated at the time of cooling after growth of the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 by th coefficient-of-thermal-expansion difference with the 1st substrate 10 decrease. Thereby, the comparatively thick IntAluGa (1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal layer 12 can be grown up to be a large area substrate. Therefore, th work which separates the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal layer 12 from the 1st substrate 10 also becomes easy compared with the case where a thin crystal layer is separated, and yield's improves.
[0114] Moreover, since the coefficient-of-thermal-expansion difference with the 1st substrate 10 is small, the defect to generate is also reduced by heat distortion compared with the case where a coefficient-of-thermal-expansion differenc uses a big substrate. Since the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal layer 17 which finally serves as a substrate grows on the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal layer 12 with few this defect, it becomes what has a few defect quality. Therefore, there are few impurities and, in addition to a crack and curvature being r duced, a low cost and a quality InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate can be further produc d by the large area.
[0115] Moreover, if the 1st substrate (single crystal substrate) 10 has th IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 and th coefficient of thermal expansion of the same grad , even if it has th laminated structure on it, it will not interfere. For example, the laminating of AlAs or the GaAs may be carried out on th GaAs substrat as th 1st substrate 10 like the after-mentioned.
[0116] Moreover, as th crystal-growth method of the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) singl crystal thin film 12, although meanses, such as MOCVD, HVPE, and MBE, are usable Especially this does not limit, and as long as it is the method of carrying out the crystal growth of the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 to the 1st substrate (single crystal substrat) 10, it may use th other methods.
[0117] Moreover, befor growing up the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film 12 The surfac

layer of the crystal lay r which did not interfere even if it deposited pr viously low-temperatur buffer layers, such as GaN. and AlN, and other layers, and grew using the 1st substrate (single crystal substrate) 10 should just be an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal.

[0118] Drawing 9 and drawing 10 are drawings showing other examples of the example of a production process shown in drawing 6 . In addition, in drawing 9 and the exampl of a process of drawing 10 , the n type GaN single crystal substrate is produced as a s miconductor substrate.

[0119] If drawing 9 and drawing 10 are referred to, first, the AlAs layer 21 and the GaAs lay r 22 will be grown epitaxially one by one by the MOCVD method on the GaAs (111) substrate 20 with a diameter of 2 inches, and let this be th 1st substrate 10. And the GaN layer 12 is grown up on this 1st substrate 10. Growth of the GaN lay r 12 is performed by the MOCVD method, ammonia and a monomethylhydrazine are used for an III group raw material by making hydrogen gas into carrier gas at 520 degrees C at trimethylgallium and V group raw material, about 25nm of GaN buffer layers 11 is deposited, and a temperature up is carried out to 750 degrees C after that, and it is made when 20 micrometers grows the GaN single crystal layer 11 (drawing 9 (a)).

[0120] Subsequently, the front face of the GaN single crystal layer 12 is pasted up on the support substrate 14 with th adhesives 13 of an organic system (drawing 9 (b-1)), subsequently to fluoric acid solution, it dips, etching removal of the AlAs layer 21 is carried out alternatively, and the GaAs substrate 20 is separated (drawing 9 (b-2)).

[0121] Subsequently, the quartz substrate 15 and the GaN single crystal layer 12 are pasted up by Ga (gallium)16 (drawing 9 (c-1)). Ga(gallium) 16 is carried on the quartz substrate 15, as the adhesion method, further, the GaAs layer 22 is made into the Ga (gallium)16 side, and is carried, and the GaN single crystal layer 12 stuck on the support substrate 14 on it is heated to the temperature beyond the melting point of Ga (gallium)16, and Ga (gallium)16 is changed into a melting state, and it pastes up.

[0122] After an appropriate time, the binder 13 of an organic system is dissolved by the organic solvent, and the support substrate 14 is separated (drawing 10 (c-2)). Temperature at this time is made below into the melting point of Ga(gallium) 16.

[0123] Subsequently, the quartz substrate 15 which pasted up the GaN single crystal layer 12 is transported to HVPE equipm nt, by making N2 gas into carrier gas, in a metal gallium and V group raw material, a silicon tetrachloride (SiCl4) is used for HCl gas and an III group raw material, and 300 micrometers grows up [in a raw material] the n type GaN single crystal 17 to be reactant gas at 1050 degrees C at ammonia gas and n type dopant gas at the front face of the GaN single crystal layer 12 (drawing 10 (d)).

[0124] Thus, it cools to 35 degrees C beyond the melting point of Ga(gallium) 16 after growth of the n type GaN single crystal 17, this temperature is held, and the quartz substrate 15 is separated (drawing 10 (e-1)). After an appropriate time, polish equipment is used, polish removal of the GaAs layer 22 and the GaN buffer layer 11 is carried out, further, polishing of the front face of the GaN single crystal layer 17 is carried out to the shape of a mirror plane, and the n type GaN single crystal substrate 17 with a thickness of about 300 micrometers is produced (drawing 10 (e-2)). Thus, an n type GaN single crystal substrate is producible as a semiconductor substrate.

[0125] In drawing 9 and the example of a production process of drawing 10 , what carried out the laminating of the AlAs lay r 21 and the GaAs layer 22 to the GaAs (111) substrate 20 one by one is used as the 1st substrate 10, and since the selection ratio of etching by the fluoric acid of AlAs and GaAs is very large, it can carry out etching removal only of the AlAs layer 21 easily. Therefore, the GaN single crystal layer 12 of a large area can be separated easily, without moreover damaging th GaAs substrate 20. Therefore, it becomes possible to produce the GaN substrate of a low cost at a large area.

[0126] In this invention, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17 produced by each production method which was mentioned above can be offered. And the conductive substrate which shows a desired conduction type can be offered by doping n type and p type dopant at the process which grows the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal 17.

[0127] That is, in this invention, the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate of the large area which a GaN system semiconductor and a coefficient-of-thermal-expansion difference are not almost, and was equipped with grid adjustment, thermal conductivity, cleavage, and conductivity can be offered.

[0128] Moreover, on the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17 produced in this invention as m ntioned above The laminating of the GaN system semiconductor laminated structure expressed with general formula InvAlwGa(1-V-W) N (0<=v<=1, 0<=w<=1, v+w<=1) containing at least one PN junction is carried out, and a semiconductor light mitting device can be offered.

[0129] Current is impressed to the electrode corresponding to p type of a semiconductor light emitting device, and n typ layer, current is poured into PN junction, and a semiconductor light emitting device emits light by the reunion of a carrier. It has at least one PN junction, and current is poured into this PN junction, and if the GaN system compound semiconductor laminated structure which constitutes a semiconductor light emitting device is structure which emits light by the reunion of a carrier, no matter they may be homozygous, a single heterojunction, a double heterojunction, quantum well structure, multiplex quantum well structure, and what other structures, it will not interfere.

[0130] Moreover, in this invention, since the cleavage was possible for the substrate, when the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17 was used for the substrate of a semiconductor light emitting device, and a semiconductor light emitting device is made into semiconductor laser, it can have a laser resonator mirror by the good cleavage of parallelism and smooth nature. Furthermor , it is possibl by making a substrate into conductivity to consider as the light emitting device which had the electrode formed in a substrate rear face (namely, thing for which n type and p typ dopant are doped to the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17).

[0131] Drawing 11 is drawing showing the example of the semiconductor light mitting d vice concerning this inv ntion. In addition, the semiconductor light emitting device of drawing 11 is constituted as semiconductor laser. If drawing 11 is referred to, this semiconductor light emitting device has the laminated structure by which the laminating of the n-GaN buffer layer 31, the n-aluminum0.15Ga0.85N clad lay r 32, the n-GaN light-guide layer 33, the In0.15Ga0.85 N/In0.02Ga0.98N multiplex quantum well structur barrier layer 34, th p-GaN light-guid lay r 35, the p-aluminum0.15Ga0.85N clad layer 36, and the p-GaN cap layer 37 was carried out one by ne on th n-GaN singl crystal substrate 17 produced by th production method which was mentioned abov .

[0132] And the ridge structure which it **********s using a remnants strike writer pattern with a width of fac of 5 micrometers from the front face of the p typ GaN cap lay r 37 of this laminated structure to the middle of the p-aluminum0.15Ga0.85N clad layer 36, and serves as a wav guide is form d. Here, the direction of a waveguide is the <1-100> direction.

[0133] Thus, th protective layer 38 which consists of SiO2 has accumulated on p-aluminum0.15Ga0.85N clad layer 36 front face exposed by forming ridge structure. Mor over, the p side ohmic electrode 39 is formed on the p-GaN cap layer 37. Moreover, the n side ohmic electrode 40 is formed in the rear face of the n-GaN singl crystal substrat 17. The optical-r sonator side of this semiconductor laser is formed by carrying out the cleavage of the field (1-100).

[0134] In the s miconductor light emitting device of drawing 11 , the crystal growth of the n-GaN buffer layer 31, the n-aluminum0.15Ga0.85N clad layer 32, the n-GaN light-guide layer 33, the In0.15Ga0.85 N/In0.02Ga0.98N multiplex quantum well structure barrier layer 34, the p-GaN light-guide layer 35, the p-aluminum0.15Ga0.85N clad layer 36, and the p-GaN cap layer 37 was carried out by the MOCVD method.

[0135] Moreover, the p side ohmic electrode 39 carried out vacuum deposition, and it is 700 degrees C in temperature, and Au/Pt/nickel was heat-treated for 20 minutes and it formed it. Moreover, the n side ohmic electrode 40 carried out vacuum d position of aluminum/Ti, heat-treated it, and formed it.

[0136] If current is impressed to the p side ohmic electrode 39 and the n side ohmic electrode 40, current is poured into the In0.15Ga0.85 N/In0.02Ga0.98N multiplex quantum well structure barrier layer 34, and the semiconductor laser of drawing 11 mits light by the reunion of a carrier, and reflective amplification will be repeated by the resonator side formed of the cleavage, and it will be outputted outside as a laser beam.

[0137] Thus, on the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate 17 produced in this invention as mentioned above Since the laminating of the GaN system semiconductor laminated structure expressed with general formula InvAlwGa(1-V-W) N (0<=v<=1, 0<=w<=1, v+w<=1) containing at least one PN junction is carried out and the semiconductor light emitting device is constituted The light emitting device which consists of a quality crystal layer by which generating of the defect by the difference in grid mismatching or a coefficient of thermal expansion was suppressed can be offered. Moreover, it is also possible to produce the semiconductor laser which has the resonator mirror formed by the light emitting device by which the electrode was formed in the substrate rear face, or the cleavage.

[0138]

[Effect of the Invention] The process which forms an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film in the 1st substrate according to invention according to claim 1 as explained above, The process at which an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal and a coefficient of thermal expansion stick an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film on the 2nd almost equivalent substrate, The process which separates an InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film from the 1st substrate, On the InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film stuck on the 2nd substrate The process which grows epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, According to the process which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrate Since an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal is produced as a semiconductor substrate There are no generating and curvature of a crack by growing up to be the big substrate of a coefficient-of-thermal-expansion difference thickly, and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate of a practical area can be produced. Moreover, since the 2nd substrate has the coefficient of thermal expansion almost equivalent to an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal Even if the crystal structure and lattice constant differ from each other, they do not interfere, its width of face of substrate selection increases by this, and they are choosing a cheap substrate and can produce an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate by the low cost.

[0139] According to invention according to claim 2, it sets to the production method of a semiconductor substrate according to claim 1. moreover, the 2nd substrate Since it is a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate There are no generating and curvature of a crack by growing up to be the big substrate of a coefficient-of-thermal-expansion difference thickly, and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate of a practical area can be produced. Moreover, since the composition element is the same, mixing of the impurity from a substrate can be reduced.

[0140] Moreover, according to invention according to claim 3, it sets to the production method of a semiconductor substrate according to claim 2. An InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film, Since all composition of a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate and an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal is the same Generating and the curvature of a crack by the coefficient-of-thermal-expansion difference are reduced further, and the InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate of a more nearly quality practical area can be produced. Moreover, since the composition element is the same, the impurity from a substrate is also reduced.

[0141] The process which forms an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film in the 1st substrate according to invention according to claim 4, The process which separates an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film from the 1st substrate, The process which sticks an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film on the 2nd substrate through a low melting point metal, On the IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film stuck on the 2nd substrate, at the temperature beyond the melting point of a low melting point metal The process which grows epitaxially an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, According to the process which separates an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from the 2nd substrat at the t mperature beyond the melting point of a low melting point metal Since an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal is produced as a semiconductor substrat The InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrat of a practical area in which a crack and curvatur were reduced is producibl by the low cost.

[0142] Moreov r, the process which forms an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) singl crystal thin film in the 1st substrate according to invention according to claim 5, Th proc ss which separates an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film from the 1st substrate, The process which sticks an IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film on th 2nd substrat through the metal Ga of a melting stat , On th IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) single crystal thin film stuck on the 2nd substrate, at the t mperatur beyond the melting point

of Metal Ga Th process made to cool without growing epitaxially an InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal, and making Metal Ga solidify, According to the process which separat s an InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal from th 2nd substrate at the temperature beyond the melting point of Metal Ga Since an InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal is produced as a semiconductor substrat There are few impurities and th InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate of a practical area in which a crack and curvatur were reduced can be produced by th low cost.

[0143] Moreover, according to invention according to claim 6, it sets to the production m thod of a semiconductor substrate according to claim 4 or 5. Sinc the 1st substrat of the above has the coefficient of thermal expansion of th same grade as an IntAluGa(1−t−u) N (0<=t<=1, 0<=u<=1, t+u<=1) singl crystal thin film An InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate with a practical quality area in which a crack and curvature were reduced is producible by the low cost.

[0144] Moreover, since it consists of an InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal produced by any 1 term of a claim 1 or a claim 6 by the production method of a publication according to invention according to claim 7 Th InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal substrate of the large area equipped with grid adjustment with a GaN system semiconductor, thermal conductivity, cleavage, and conductivity can be offered.

[0145] According to invention according to claim 8, moreover, on the semiconductor substrate of the InxAlyGa(1−x−y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal of a claim 7 Since the laminating of the GaN system semiconductor laminated structure expressed with general formula InvAlwGa(1−V−W) N (0<=v<=1, 0<=w<=1, v+w<=1) containing at least one PN junction is carried out and it is constituted, the semiconductor light emitting device which consists of a quality crystal layer in which the defect was reduced can be offered. Moreover, an electrode is formed in a substrate rear face and the semiconductor laser which has a resonator mirror by the cleavage can be offered.

[Translation done.]

* NOTICES *

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damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In th drawings, any words are not translat d.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the example of a production process of the semiconductor substrate concerning this invention.
[Drawing 2] It is drawing showing the example of the example of a production process of the semiconductor substrate shown in drawing 1 .
[Drawing 3] It is drawing showing the example of a production process in the case of using the 2nd substrate as a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate.
[Drawing 4] An InrAlsGa(1-r-s) N (0<=r<=1, 0<=s<=1, r+s<=1) single crystal thin film, It is drawing showing the example of a production process in the case of making the same all composition of a polycrystal IntAluGa(1-t-u) N (0<=t<=1, 0<=u<=1, t+u<=1) substrate and an InxAlyGa(1-x-y) N (0<=x<=1, 0<=y<=1, x+y<=1) single crystal.
[Drawing 5] It is drawing showing the example of the semiconductor light emitting device concerning this invention.
[Drawing 6] It is drawing showing the example of a production process of the semiconductor substrate concerning this invention.
[Drawing 7] It is drawing showing the example of the example of a production process of the semiconductor substrate shown in drawing 6 .
[Drawing 8] It is drawing showing the example of the example of a production process of the semiconductor substrate shown in drawing 6 .
[Drawing 9] It is drawing showing the example of the example of a production process of the semiconductor substrate shown in drawing 6 .
[Drawing 10] It is drawing showing the example of the example of a production process of the semiconductor substrate shown in drawing 6 .
[Drawing 11] It is drawing showing the example of the semiconductor light emitting device concerning this invention.
[Drawing 12] It is drawing showing the conventional semiconductor laser.
[Drawing 13] It is drawing showing the conventional semiconductor laser.
[D scription of Notations]
10 1st Substrate (Single Crystal Substrate)
11 GaN Buffer Layer
12 IntAluGa(1-T-u) N (0<=T<=1, 0<=U<=1, T+u<=1) Single Crystal Thin Film
13 Adhesives of Organic System
14 Support Substrate
15 2nd Substrate
16 Low Melting Point Metal (Indium or Gallium)
17 InxAlyGa(1-X-y) N (0<=X<=1, 0<=Y<=1, X+y<=1) Single Crystal Substrate
20 (111) GaAs Substrate
21 AlAs Layer
22 GaAs Layer
31 N-GaN Buffer Layer
32 N-aluminum0.15Ga0.85N Clad Layer
33 N-GaN Light-Guide Layer
34 In0.15Ga0.85 N/In0.02Ga0.98N Multiplex Quantum Well Structure Barrier Layer
35 P-GaN Light-Guide Layer
36 P-aluminum0.15Ga0.85N Clad Layer
37 P-GaN Cap Layer
38 Protective Layer Which Consists of SiO2
39 The P Side Ohmic Electrode
40 The N Side Ohmic Electrode
50 1st Substrate (Single Crystal Substrate)
51 GaN Buffer Layer
52 InrAlsGa(1-R-s) N (0<=R<=1, 0<=S<=1, R+s<=1) Single Crystal Thin Film
53 2nd Substrate
54 InxAlyGa(1-X-y) N (0<=X<=1, 0<=Y<=1, X+y<=1) Single Crystal
111 (0001) Silicon on Sapphire
112 N Typ GaN Low-temperature Buffer Layer
113,132 Elevated-temperature buffer layer which consists of n type GaN
114 SiO2 Selective-Growth Mask
115,133 n-In0.1Ga0.9N crack prevention layer
116,134 n-aluminum0.14Ga0.86 N/GaN MD-SLS (modulation dope strain d super lattice) clad layer
117,135 n-GaN light-guide layer
118,136 In0.15Ga0.86 N/In0.02Ga0.98N MQW barri r layer

120,138 p-GaN layer light-guide layer
121,139 p-aluminum0.14Ga0.86 N/GaN MD-SLS clad layer
122,140 p type GaN layer cap layer
123,143 P lateral electrode
124,142 SiO2 protectiv layer
125,141 n lateral electrode
131 (0001) Field GaN Substrate

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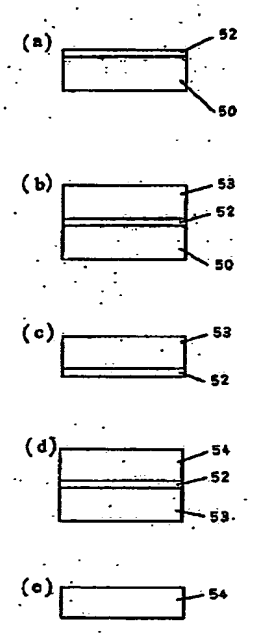
(54)【発明の名称】　半導体基板およびその作製方法および半導体発光素子

(57)【要約】
【課題】　工業的に実用化できる大面積，高品質のＧａＮ系の半導体基板およびその作製方法および半導体発光素子を提供する。
【解決手段】　第１の基板５０に$In_rAl_sGa_{(1-r-s)}N$(0≦r≦1，0≦s≦1，r＋s≦1)単結晶薄膜５２を形成し、$In_rAl_sGa_{(1-r-s)}N$単結晶薄膜５２を$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶と熱膨張係数がほぼ同等である第２の基板５３に貼り付け、第１の基板５０から$In_rAl_sGa_{(1-r-s)}N$単結晶薄膜５２を分離し、第２の基板５３に貼り付けられた$In_rAl_sGa_{(1-r-s)}N$単結晶薄膜５２上に、$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶５４をエピタキシャル成長し、第２の基板５３から$In_xAl_yGa_{(1-x-y)}N$単結晶５４を分離する。



【特許請求の範囲】

【請求項１】 第１の基板に$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜を形成する工程と、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜を$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶と熱膨張係数がほぼ同等である第２の基板に貼り付ける工程と、第１の基板から$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜を分離する工程と、第２の基板に貼り付けられた$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜上に、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶をエピタキシャル成長する工程と、第２の基板から$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を半導体基板として作製することを特徴とする半導体基板の作製方法。

【請求項２】 請求項１記載の半導体基板の作製方法において、第２の基板は、多結晶$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）基板であることを特徴とする半導体基板の作製方法。

【請求項３】 請求項２記載の半導体基板の作製方法において、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜、多結晶$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）基板、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶の組成がすべて同一であることを特徴とする半導体基板の作製方法。

【請求項４】 第１の基板に$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を形成する工程と、第１の基板から$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を分離する工程と、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を低融点金属を介して第２の基板に貼り付ける工程と、第２の基板に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜上に、低融点金属の融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶をエピタキシャル成長する工程と、第２の基板から$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を低融点金属の融点以上の温度で分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を半導体基板として作製することを特徴とする半導体基板の作製方法。

【請求項５】 第１の基板に$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を形成する工程と、第１の基板から$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を分離する工程と、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を溶融状態の金属Ｇａを介して第２の基板に貼り付ける工程と、第２の基板に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜上に、金属Ｇａの融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶をエピタキシャル成長し、金属Ｇａを凝固させずに冷却させる工程と、第２の基板から$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を金属Ｇａの融点以上の温度で分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を半導体基板として作製することを特徴とする半導体基板の作製方法。

【請求項６】 請求項４または請求項５記載の半導体基板の作製方法において、前記第１の基板は$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜と同程度の熱膨張係数を有していることを特徴とする半導体基板の作製方法。

【請求項７】 請求項１乃至請求項６のいずれか一項に記載の作製方法によって作製された$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶からなることを特徴とする半導体基板。

【請求項８】 請求項７の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶の半導体基板上に、少なくとも一つのP-N接合を含む一般式$In_vAl_wGa_{(1-v-w)}N$（$0 \leqq v \leqq 1$，$0 \leqq w \leqq 1$，$v+w \leqq 1$）で表わされるＧａＮ系半導体積層構造が積層されて構成されていることを特徴とする半導体発光素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＤＶＤやＣＤ等の光ピックアップ用光源などに利用される半導体基板およびその作製方法および半導体発光素子に関する。

【０００２】

【従来の技術】従来、青色のＬＥＤは赤色や緑色に比べて輝度が小さく実用化に難点があったが、近年、一般式ＩｎＡｌＧａＮで表わされるＧａＮ系化合物半導体において、低温ＡｌＮバッファ層、あるいは低温ＧａＮバッファ層を用いることによる結晶成長技術の向上と、Ｍｇをドープした低抵抗のｐ型半導体層が得られたことにより、高輝度の青色ＬＥＤが実用化され、さらには、実用化には至らないが室温で連続発振する半導体レーザが実現された。

【０００３】ところで、一般に、高品質の半導体層を基板上にエピタキシャル成長させる場合には、基板と半導体層の格子定数や熱膨張係数が同程度である必要がある。しかし、ＧａＮ系半導体はこれらを同時に満足する基板が現時点では存在しない。現在、ＧａＮバルク単結晶を作製する試みがなされているが、いまだに数ミリ程

度のものしか得られていないのが実状であり、実用化には程遠い状態である。従って、一般には、サファイア，$MgAl_2O_4$ スピネル，ＳｉＣのようなＧａＮ系半導体とは格子定数や熱膨張係数の大きく異なる基板の上に成長されている。そのため、ＧａＮ系半導体では、高品質の結晶層を必要とする半導体レーザの作製のために、基板と半導体レーザ結晶との格子定数や熱膨張係数の違いに起因する結晶欠陥の発生を抑制する技術が用いられている。

【０００４】図１２は文献「Applied Physics Letters Vol.72(1998)P.211」に示されている従来の端面発光型半導体レーザの断面図であり、図１２の半導体レーザも上述のような技術が用いられたものの一つである。図１２に示す従来の半導体レーザは、選択成長とラテラル成長を組み合わせて作製される低欠陥基板上に形成されている。

【０００５】すなわち、図１２の半導体レーザは次のような方法で作製されている。先ず、厚さ１００～３００μｍの(０００１)面を主面とするサファイア(Al_2O_3単結晶)基板１１１上に、ｎ型ＧａＮからなる低温バッファ層１１２，ｎ型のＧａＮからなる高温バッファ層１１３を成長する。次いで、ｎ型ＧａＮ層１１３の表面にSiO_2を堆積し、ストライプ状のパターンを開け、選択成長マスク１１４を形成する。次に、このマスクから露出したＧａＮ層１１３の表面にＧａＮを選択成長させる。そしてさらに、成長を継続して、マスク表面上へのラテラル成長を行ない、最終的に厚さ約２０μｍのｎ型ＧａＮ単結晶層を形成し、半導体レーザ結晶成長用基板としている。

【０００６】そして、半導体レーザ構造は、ｎ－$In_{0.1}Ga_{0.9}N$クラック防止層１１５，ｎ－$Al_{0.14}Ga_{0.86}N$／ＧａＮ ＭＤ－ＳＬＳ(モジュレーションドープ歪み超格子)クラッド層１１６，ｎ－ＧａＮ光ガイド層１１７，$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$ ＭＱＷ活性層１１８，ｐ－$Al_{0.2}Ga_{0.8}N$転位伝播防止層１１９，ｐ－ＧａＮ層光ガイド層１２０，ｐ－$Al_{0.14}Ga_{0.86}N$／ＧａＮＭＤ－ＳＬＳクラッド層１２１，ｐ型ＧａＮ層からなるキャップ層１２２がＭＯＣＶＤ法により順次積層されている。この積層された半導体層をリッジ状にドライエッチングすることによって、光導波路と光共振器端面が形成され、さらに、エッチングにより露出したｎ－ＧａＮ層１１３および積層された半導体層の表層であるキャップ層１２２にそれぞれｎ側電極１２５およびｐ側電極１２３が設けられることにより、半導体レーザが形成されている。

【０００７】図１２に示した選択成長とラテラル成長を組み合わせて作製される低欠陥基板上への半導体レーザ形成技術の開発により、半導体レーザの室温連続発振の寿命も室温近傍で、低出力ながら推定１００００時間程度まで延びている。具体的に、このような構造のＧａＮ系半導体レーザによって、２０℃、２ｍＷでの連続発振の寿命は推定１００００時間程度まで延びている。

【０００８】しかしながら、図１２のような従来のＧａＮ系化合物半導体層を使用した発光素子は、結晶構造の異なる異種基板に成長するため、基板とＧａＮ系化合物半導体のへき開面が必ずしも一致しているわけではなく、レーザ共振器端面の形成を従来のＡｌＧａＡｓ系等のレーザようなへき開法で行なうことが困難である。

【０００９】図１２の従来例では、光共振器端面はドライエッチングなどの方法で作製している。そのため、作製プロセスもドライエッチング用マスクの形成、ドライエッチング、マスクの除去等の工程が必要とされ複雑化していた。さらにはＧａＮ系化合物半導体のドライエッチング技術は未だ確立されていないため、形成された共振器ミラーには、縦筋状の凹凸があり、また、テーパー状に形成されるなど、その平滑性、平行性、垂直性は未だ十分ではなかった。また、ドライエッチングで共振器ミラーを形成した場合には、共振器ミラー端面の前方に基板がテラスとして残るため、このテラスによって、光が反射され、ビーム形状が単峰にならなかった。

【００１０】また、サファイア基板上に形成された従来のＧａＮ系化合物半導体を使用した発光素子は、サファイア基板が絶縁性であるため、基板裏面から電極をとることができなかった。そのため、電極は素子表面に形成されることになり、従来のＡｌＧａＡｓ系等のレーザのように基板裏面に電極を形成しダイボンディングするような実装ができない上、電極のスペースの分だけチップ面積が大きくなるといった問題も残っていた。また、サファイア基板の熱伝導性の悪さから、高温動作、あるいは、大出力動作では、寿命は極端に短かった。

【００１１】サファイア基板以外の基板でのＧａＮ系レーザ素子について、(０００１)ｃ面ＳｉＣ基板と(１１１)$MgAl_2O_4$基板を用いる場合が報告されているが、ＳｉＣ基板を用いる場合には、ＳｉＣとＧａＮ系半導体の熱膨張係数の違いから結晶成長時にクラックが入り、レーザ構造として十分な厚さの積層構造の形成が困難であり、室温連続発振には至っていない。また、(１１１)$MgAl_2O_4$基板を用いる場合には、サファイアと同様に絶縁性であるため、基板裏面に電極を形成することができない。

【００１２】このような異種材料基板に作製されたＧａＮ系半導体レーザの問題点を解決すべく、サファイア基板上に結晶成長したＧａＮ系半導体層を基板から分離してＧａＮ基板を作製し、ＧａＮ系半導体レーザを作製した報告もなされている。

【００１３】図１３は、文献「Jpn.J.Appl.Phys.Vol.37 (1998)pp.L309-L312」に示されている従来の端面発光型半導体レーザの断面図であり、図１３の半導体レーザは、図１２と同様の構造のレーザ構造がＧａＮ基板上に形成されたものである。

【００１４】すなわち、図１３の半導体レーザは、（０００１）面を主面とするＧａＮからなる８０μｍの厚さの基板１３１上に、ｎ型のＧａＮからなる高温バッファ層１３２，ｎ－$In_{0.1}Ga_{0.9}N$クラック防止層１３３，ｎ－$Al_{0.14}Ga_{0.86}N$／ＧａＮ　ＭＤ－ＳＬＳ（モジュレーションドープ歪み超格子）クラッド層１３４，ｎ－ＧａＮ光ガイド層１３５，$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$　ＭＱＷ活性層１３６，ｐ－$Al_{0.2}Ga_{0.8}N$転位伝播防止層１３７，ｐ－ＧａＮ層光ガイド層１３８，ｐ－$Al_{0.14}Ga_{0.86}N$／ＧａＮ　ＭＤ－ＳＬＳクラッド層１３９，ｐ型ＧａＮ層からなるキャップ層１４０がＭＯＣＶＤ法により順次積層されている。この積層された半導体層をリッジ状にドライエッチングすることによって、光導波路が形成され、さらに、エッチングにより露出したｎ－ＧａＮ層１３２および積層された半導体層の表層であるキャップ層１４０にそれぞれｎ側電極１４３およびｐ側電極１４１が設けられることにより、半導体レーザが形成されている。レーザの共振器ミラーはへき開によって作製されている。

【００１５】このように、図１３のＧａＮ基板は、図１２に示した半導体レーザの低欠陥基板上に、半導体レーザの積層構造１１５～１２２の代わりにＧａＮ層を約１００μｍ成長したものを作製し、その後、サファイア基板を研磨除去して、８０μｍの厚さのＧａＮ基板として作製されている。

【００１６】また、図１３に示した端面発光型半導体レーザは、ＧａＮ基板上に形成されているので、共振器ミラーの形成はへき開で行なうことができる。その結果、基板での反射がなく、ビーム形状は単峰となった。また、サファイア基板に比べ、熱伝導率が高いので、放熱特性が向上し、高出力動作が可能となり、寿命は５０℃、３０ｍＷ動作でも、２５０時間まで延びている。

【００１７】図１３の例のように、単結晶基板上にＧａＮ系半導体を厚く成長した後、基板からＧａＮ系半導体層を分離し、ＧａＮ系半導体基板を作製する方法はいくつか提案されている。例えば、特開平７－２０２２６５号公報，特開平７－１６５４９８号には、サファイア基板上に、ＺｎＯよりなるバッファ層を形成し、その上にＧａＮ系半導体を成長させた後、バッファ層を溶解除去し、基板とＧａＮ系半導体とを分離して作製する方法が開示されている。

【００１８】また、特開平１０－２２９２１８号には、第１の基板上にＧａＮ系半導体が成長された第１のウエハーと、第２の基板上にＧａＮ系半導体が成長された第２のウエハーとを用意し、第１のウエハーと第２のウエハーとをそれぞれのＧａＮ系半導体同士が密着するようにして接着した後、第１の基板と第２の基板とを研磨除去する方法が開示されている。

【００１９】

【発明が解決しようとする課題】前述のように、低温バッファ層の技術や選択成長とラテラル成長の組み合わせによる低欠陥基板の作製技術により、サファイア等の異種基板上への高品質ＧａＮ系化合物半導体の結晶成長が可能となり、ＧａＮ系半導体レーザの室温近傍での低出力動作時の長寿命化が図られた。さらには、ＧａＮ基板が作製され、この基板を用いることによりＧａＮ系半導体レーザの特性の改善が見込まれつつある。しかるに、工業的に実用化できる大面積，高品質のＧａＮ基板は未だ実現されていない。

【００２０】図１３に示したＧａＮ基板の作製方法では、ＧａＮとサファイア基板との熱膨張係数差により、厚いＧａＮを成長するとウエハーの反りが生じるため、直径が２インチ程度のサファイア基板を研磨除去することは困難である。すなわち従来のような基板の研磨除去の方法では、大面積のＧａＮ基板を作製することは困難であった。また、この反りのためにサファイア基板研磨の過程で、ＧａＮ層に欠陥が導入されるなどして、結晶性が悪くなり、その上に作製した半導体レーザのしきい電流密度が増加するなど、半導体レーザの特性は必ずしも良いものではなかった。

【００２１】また、特開平１０－２２９２１８号に開示されている第１のウエハーと第２のウエハーとをそれぞれのＧａＮ系半導体同士が密着するようにして接着した後、第１の基板と第２の基板とを除去する方法では、基板とＧａＮ系半導体との熱膨張係数の違いによってＧａＮを厚く成長するとウエハーが反るため、大面積のウエハーでは、ウエハー全面でＧａＮ系半導体同士が完全に密着しないこともある。また、密着の過程でクラックが入る場合もある。さらに、第１の基板と第２の基板を研磨除去するため、１枚のＧａＮ基板を作製するのに２枚の高価な基板を使うことになり高コストになるなどの問題もあった。

【００２２】また、特開平７－２０２２６５号，特開平７－１６５４９８号に示されている技術，すなわち、基板の研磨除去を要しないＧａＮ基板を作製する技術では、薄膜のＺｎＯよりなるバッファ層を溶解除去するのに非常に長時間を要し、実用化は難しかった。

【００２３】本発明は、このような従来のＧａＮ系半導体基板の作製方法の問題点を解決し、工業的に実用化できる大面積，高品質のＧａＮ系の半導体基板およびその作製方法および半導体発光素子を提供することを目的としている。

【００２４】

【課題を解決するための手段】上記目的を達成するために、請求項１記載の発明は、第１の基板に$In_rAl_sGa_{(1-r-s)}N$（$0\leq r\leq 1$，$0\leq s\leq 1$，$r+s\leq 1$）単結晶薄膜を形成する工程と、$In_rAl_sGa_{(1-r-s)}N$（$0\leq r\leq 1$，$0\leq s\leq 1$，$r+s\leq 1$）単結晶薄膜を$In_xAl_yGa_{(1-x-y)}N$（$0\leq x\leq 1$，$0\leq y\leq 1$，$x+y\leq 1$）単結晶と熱膨張係数がほぼ同等である第２の基

板に貼り付ける工程と、第1の基板から$In_rAl_sGa_{(1-r-s)}N$($0\leqq r\leqq 1$，$0\leqq s\leqq 1$，$r+s\leqq 1$)単結晶薄膜を分離する工程と、第2の基板に貼り付けられた$In_rAl_sGa_{(1-r-s)}N$($0\leqq r\leqq 1$，$0\leqq s\leqq 1$，$r+s\leqq 1$)単結晶薄膜上に、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶をエピタキシャル成長する工程と、第2の基板から$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶を分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶を半導体基板として作製することを特徴としている。

【0025】また、請求項2記載の発明は、請求項1記載の半導体基板の作製方法において、第2の基板は、多結晶$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)基板であることを特徴としている。

【0026】また、請求項3記載の発明は、請求項2記載の半導体基板の作製方法において、$In_rAl_sGa_{(1-r-s)}N$($0\leqq r\leqq 1$，$0\leqq s\leqq 1$，$r+s\leqq 1$)単結晶薄膜、多結晶$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)基板、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶の組成がすべて同一であることを特徴としている。

【0027】請求項4記載の発明は、第1の基板に$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜を形成する工程と、第1の基板から$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜を分離する工程と、$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜を低融点金属を介して第2の基板に貼り付ける工程と、第2の基板に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜上に、低融点金属の融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶をエピタキシャル成長する工程と、第2の基板から$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶を低融点金属の融点以上の温度で分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶を半導体基板として作製することを特徴としている。

【0028】また、請求項5記載の発明は、第1の基板に$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜を形成する工程と、第1の基板から$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜を分離する工程と、$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜を溶融状態の金属Gaを介して第2の基板に貼り付ける工程と、第2の基板に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜上に、金属Gaの融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶をエピタキシャル成長し、金属Gaを凝固させずに冷却させる工程と、第2の基板から$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶を金属Gaの融点以上の温度で分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶を半導体基板として作製することを特徴としている。

【0029】また、請求項6記載の発明は、請求項4または請求項5記載の半導体基板の作製方法において、前記第1の基板は$In_tAl_uGa_{(1-t-u)}N$($0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$)単結晶薄膜と同程度の熱膨張係数を有していることを特徴としている。

【0030】また、請求項7記載の発明は、半導体基板が、請求項1乃至請求項6のいずれか一項に記載の作製方法によって作製された$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶からなることを特徴としている。

【0031】また、請求項8記載の発明は、半導体発光素子が、請求項7の$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶の半導体基板上に、少なくとも一つのP-N接合を含む一般式$In_vAl_wGa_{(1-v-w)}N$($0\leqq v\leqq 1$，$0\leqq w\leqq 1$，$v+w\leqq 1$)で表わされるGaN系半導体積層構造が積層されて構成されていることを特徴としている。

【0032】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。図1は本発明に係る半導体基板の作製工程例を示す図である。図1の作製工程例では、

a．第1の基板（単結晶基板）50に$In_rAl_sGa_{(1-r-s)}N$($0\leqq r\leqq 1$，$0\leqq s\leqq 1$，$r+s\leqq 1$)単結晶薄膜52を形成する工程（図1（a））と、

b．$In_rAl_sGa_{(1-r-s)}N$($0\leqq r\leqq 1$，$0\leqq s\leqq 1$，$r+s\leqq 1$)単結晶薄膜52を$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶と熱膨張係数がほぼ同等である第2の基板53に貼り付ける工程（図1（b））と、

c．第1の基板(単結晶基板)50から$In_rAl_sGa_{(1-r-s)}N$($0\leqq r\leqq 1$，$0\leqq s\leqq 1$，$r+s\leqq 1$)単結晶薄膜52を分離する工程（図1（c））と、

d．第2の基板53に貼り付けられた$In_rAl_sGa_{(1-r-s)}N$($0\leqq r\leqq 1$，$0\leqq s\leqq 1$，$r+s\leqq 1$)単結晶薄膜52上に、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶54をエピタキシャル成長する工程（図1（d））と、

e．第2の基板53から$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶54を分離する工程（図1（e））とを有し、最終的に、$In_xAl_yGa_{(1-x-y)}N$($0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$)単結晶基板54を作製するようになっている。

【0033】ここで、第1の基板(単結晶基板)50とし

ては、サファイア（０００１）c面、サファイア（１１－２０）a面、$MaAl_2O_4$スピネル（１１１）面、６Ｈ－ＳｉＣ（０００１）c面、６Ｈ－ＳｉＣ（１－１００）m面等が使用可能である。

【００３４】また、aの工程において、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜５２の結晶成長方法としては、ＭＯＣＶＤ，ＨＶＰＥ，ＭＢＥ等の手段が使用可能であるが、上記方法に限定されるものではなく、第１の基板（単結晶基板）５０に、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜５２を結晶成長させることができる方法であれば、その他の方法を用いても良い。また、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜５２を成長する際に、ＧａＮやＡｌＮ等の低温バッファ層を先に堆積しても差し支えなく、第１の基板（単結晶基板）１０を使用して成長した結晶層の表面層が$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶であれば良い。

【００３５】また、bの工程において、第２の基板５３としては、単結晶あるいは、多結晶のモリブデン基板（$6 \times 10^{-6}k^{-1}$），単結晶$YAlO_3$基板，単結晶ＧＧＧ（$Gd_3Ga_5O_{12}$）基板、あるいは、熱膨張係数が$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶５４と同程度になるように原料組成を調節して作製された単結晶あるいは、多結晶あるいは非晶質体等が使用可能である。

【００３６】また、第２の基板５３に貼り付ける方法としては、窒化物半導体の分解圧以上に加圧された窒素雰囲気中でウエハを加熱し、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜５２と第２の基板５３とを拡散接合で直接接着することが可能であるが、cの工程での第１の基板５０の除去や、dの工程での$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶５４をエピタキシャル成長するのに支障の無い方法であれば、その他の方法であっても差し支えない。

【００３７】また、貼り付けの程度は、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜５２の表面全面が、第２の基板５３に完全に接合されている必要はなく、cの工程での第１の基板５０の除去やdの工程での$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶５４をエピタキシャル成長するのに支障の無い程度であれば、部分的に接合されている程度でも差し支えない。また、その接合強度も、cの工程での第１の基板５０の除去やdの工程における$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶５４をエピタキシャル成長するのに支障の無ければ、弱くても差し支えない。

【００３８】また、cの工程において、第１の基板（単結晶基板）５０を$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜５２から分離する方法としては、化学エッチング，研磨等が使用可能であるが、特に限定されるものではなく、適宜使用可能である。

【００３９】また、dの工程において、第２の基板５３に貼り付けられた$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜５２上に、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶５４をエピタキシャル成長する方法としては、特に限定されるものではないが、厚い単結晶層を成長することから、ＨＶＰＥ法や高速のＭＯＣＶＤ法等の成長速度の速い方法が望ましい。また、ｎ型やｐ型ドーパントをドープすることにより、伝導型を制御することが可能である。

【００４０】また、eの工程において、第２の基板５３から$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶５４を分離する方法としては、化学エッチング，研磨等が使用可能であるが、特に限定されるものではなく、適宜可能である。

【００４１】図２は図１に示した作製工程例の具体例を示す図である。図２の工程例では、半導体基板として、ｎ型ＧａＮ単結晶基板を作製している。

【００４２】図２を参照すると、先ず、直径２インチの（０００１）c面サファイア基板５０上に、５２０℃で水素ガスをキャリアガスとして、III族原料にトリメチルガリウム、Ｖ族原料にアンモニウムを使用して、ＧａＮバッファ層５１を約２５ｎｍ堆積し、その後、１０５０℃に昇温し、ＧａＮ単結晶層５２を８μｍ成長する（図２（ａ））。

【００４３】次いで、表面をポリッシングして鏡面状にした多結晶Ｍｏ基板５３とＧａＮ単結晶５２の表面を密着させ、耐熱性の治具で強く固定した状態で、アニール装置に移送する。そして、窒素雰囲気中２０気圧、１１００℃において、アニールを行い、両者を拡散接合させる（図２（ｂ））。

【００４４】次いで、研磨装置を使用して、サファイア（０００１）基板５０を研磨除去する（図２（ｃ））。この時、ＧａＮバッファ層５１は低温で成長した多結晶層を含む層であるので同時に研磨除去し、さらに、露出したＧａＮ単結晶層５２の表面を鏡面状にポリッシングする。

【００４５】次いで、Ｍｏ基板５３をＨＶＰＥ装置に移送し、N_2ガスをキャリアガスとして、反応ガスにＨＣｌガス、III族原料に金属ガリウム、Ｖ族原料にアンモニアガス、ｎ型ドーパントガスに四塩化珪素（$SiCl_4$）を使用して、１０５０℃で露出したＧａＮ単結晶層５２の表面にｎ型ＧａＮ単結晶５４を３００μｍ成長する（図２（ｄ））。

【００４６】次いで、研磨装置を使用して、Ｍｏ基板５３を研磨除去する。さらに、露出したＧａＮ単結晶層５

4の表面を鏡面状にポリッシングし、厚さ300μmのn型GaN単結晶基板54を作製する(図2(e))。このようにして、半導体基板として、n型GaN単結晶基板を作製することができる。

【0047】図1，図2の作製工程例では、上述の工程をとることによって、熱膨張係数差の大きな基板50に厚く成長することによるクラックの発生や反りがなく、実用的な面積の$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶基板54が作製される。また、第2の基板53は、熱膨張係数が$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶54とほぼ同等であれば、その結晶構造や格子定数は異なっても差し支えないので、基板選択の幅が増え、安価な基板を選択することで、低コストで$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶基板54が作製される。

【0048】ところで、上述の図1，図2の作製方法では、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶54と異なる材料からなる第2の基板53を使用した場合、第2の基板の融点や化学的安定性によって、結晶成長温度や成長雰囲気といった結晶成長条件に制約がつく場合があった。また、第2の基板53の構成元素が$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶54中へ不純物として拡散する懸念もあった。

【0049】このような問題を回避するためには、第2の基板53を、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶層54と同種の材料からなる多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板とするのが良い。すなわち、第2の基板53を多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板にするのが良い。

【0050】図3は第2の基板53を多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板にする場合の作製工程例を示す図である。なお、図3の例では、半導体基板として、n型$In_{0.1}Ga_{0.9}N$単結晶基板を作製している。

【0051】図3を参照すると、先ず、直径2インチの(0001)c面サファイア基板50上に、520℃で水素ガスをキャリアガスとして、III族原料にトリメチルガリウム、V族原料にアンモニウムを使用して、GaNバッファ層51を約25nm堆積し、その後、1050℃に昇温し、GaN単結晶層52を8μm成長する(図3(a))。

【0052】次いで、表面をポリッシングして鏡面状にした多結晶GaN基板53とGaN単結晶層52の表面を密着させ(図3(b))、耐熱性の治具で強く固定した状態で、アニール装置に移送する。そして、窒素雰囲気中20気圧、1100℃において、アニールを行い、両者を拡散接合させる。

【0053】次いで、研磨装置を使用して、サファイア(0001)基板50を研磨除去する。この時、GaNバッファ層51は低温で成長した多結晶層を含む層であるので同時に研磨除去し、さらに、露出したGaN単結晶層52の表面を鏡面状にポリッシングする(図3(c))。

【0054】次いで、多結晶GaN基板53をMOVPE装置に移送し、N_2ガスをキャリアガスとして、III族原料にトリメチルガリウム，トリメチルインジウム、V族原料にアンモニアガス，モノメチルヒドラジン、n型ドーパントガスにモノシランを使用して、800℃で露出したGaN単結晶層52の表面にn型$In_{0.1}Ga_{0.9}N$単結晶54を200μm成長する(図3(d))。

【0055】次いで、研磨装置を使用して、多結晶GaN基板53を研磨除去する。さらに、露出したGaN単結晶層54の表面を鏡面状にポリッシングし、厚さ約200μmのn型$In_{0.1}Ga_{0.9}N$単結晶基板54を作製する(図3(e))。

【0056】このように、図3の工程例によれば、第2の基板53が多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板であるので、熱膨張係数差の大きな基板に厚く成長することによるクラックの発生や反りがなく、実用的な面積の$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶基板54が作製される。また、構成元素が同一であるので、基板からの不純物の混入が低減される。

【0057】ところで、図3の作製工程例では、第2の基板53に$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶層54と同種の材料からなる多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板を使用することによって、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶層54の成長条件の第2の基板53による制約をなくし、基板53の構成元素が不純物として混入する懸念を低減したが、多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板53は、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶層とは混晶組成が異なっているので、第2の基板53と$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶層54とでは、熱膨張係数が異なる。従って、熱膨張係数差に起因する熱歪みのため欠陥が発生することが懸念される。

【0058】このような問題を回避するためには、図3の作製工程例において、$In_rAl_sGa_{(1-r-s)}N$($0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$)単結晶薄膜52、多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板53、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶54の組成をすべて同一にして、第2の基板53と結晶層54の

熱膨張係数差をほぼゼロにして、熱歪みによる欠陥の発生を低減するのが良い。

【００５９】図４は$In_rAl_sGa_{(1-r-s)}N$($0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$)単結晶薄膜５２、多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板５３、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶５４の組成をすべて同一にする場合の作製工程例を示す図である。なお、図４の例では、半導体基板として、n型$Al_{0.15}Ga_{0.85}N$単結晶基板を作製している。

【００６０】図４を参照すると、先ず、直径２インチの（０００１）c面サファイア基板５０上に、５２０℃で水素ガスをキャリアガスとして、III族原料にトリメチルガリウム、V族原料にアンモニウムを使用して、$Al_{0.15}Ga_{0.85}N$バッファ層５１を約２５ｎｍ堆積し、その後、１０５０℃に昇温し、$Al_{0.15}Ga_{0.85}N$単結晶層５２を８μm成長する（図４(a)）。

【００６１】次いで、表面をポリッシングして鏡面状にした多結晶$Al_{0.15}Ga_{0.85}N$基板５３と$Al_{0.15}Ga_{0.85}N$単結晶５２の表面を密着させ（図４(b)）、耐熱性の治具で強く固定した状態で、アニール装置に移送する。そして、窒素雰囲気中２０気圧、１１００℃において、アニールを行い、両者を拡散接合させる。

【００６２】次いで、研磨装置を使用して、サファイア（０００１）基板５０を研磨除去する。この時、$Al_{0.15}Ga_{0.85}N$バッファ層５１は低温で成長した多結晶層を含む層であるので同時に研磨除去し、さらに、露出した$Al_{0.15}Ga_{0.85}N$単結晶層５２の表面を鏡面状にポリッシングする（図４(c)）。

【００６３】次いで、$Al_{0.15}Ga_{0.85}N$基板５３をMOVPE装置に移送し、H_2ガスをキャリアガスとして、III族原料にトリメチルガリウム、トリメチルアルミニウム、V族原料にアンモニアガス、n型ドーパントガスにモノシランを使用して、１０５０℃で露出した$Al_{0.15}Ga_{0.85}N$単結晶層５２の表面にn型$Al_{0.15}Ga_{0.85}N$単結晶５４を３００μm成長する（図４(d)）。

【００６４】次いで、研磨装置を使用して、多結晶$Al_{0.15}Ga_{0.85}N$基板５３を研磨除去する。さらに、露出した$Al_{0.15}Ga_{0.85}N$単結晶層５４の表面を鏡面状にポリッシングし、厚さ３００μmのn型$Al_{0.15}Ga_{0.85}N$単結晶基板５４を作製する（図４(e)）。

【００６５】上述の例では、半導体基板として、n型$Al_{0.15}Ga_{0.85}N$単結晶基板を作製する例を示したが、他の例として、n型GaN単結晶基板を作製することもできる。n型GaN単結晶基板を作製する方法を、便宜上、前述した図４を用いてて説明する。

【００６６】半導体基板として、n型GaN単結晶基板を作製する場合、先ず、直径２インチの（０００１）c面サファイア基板５０上に、５２０℃で水素ガスをキャリアガスとして、III族原料にトリメチルガリウム、V族原料にアンモニウムを使用して、GaNバッファ層５１を約２５ｎｍ堆積し、その後、１０５０℃に昇温し、GaN単結晶層５２を８μm成長する（図４(a)）。

【００６７】次いで、多結晶GaN基板３３とGaN単結晶３２の表面を密着させ（図４(b)）、耐熱性の治具で強く固定した状態で、アニール装置に移送する。そして、窒素雰囲気中２０気圧、１１００℃において、アニールを行い、両者を拡散接合させる。

【００６８】次いで、研磨装置を使用して、サファイア（０００１）基板５０を研磨除去する。この時、GaNバッファ層５１は低温で成長した多結晶層を含む層であるので同時に研磨除去し、さらに、露出したGaN単結晶層５２の表面を鏡面状にポリッシングする（図４(c)）。

【００６９】次いで、多結晶GaN基板５３をHVPE装置に移送し、N_2ガスをキャリアガスとして、反応ガスにHClガス、III族原料に金属ガリウム、V族原料にアンモニアガス、n型ドーパントガスに四塩化珪素（$SiCl_4$）を使用して、１０５０℃で露出したGaN単結晶層５２の表面にn型GaN単結晶５４を３００μm成長する（図４(d)）。

【００７０】次いで、研磨装置を使用して、多結晶GaN基板５３を研磨除去する。さらに、露出したGaN単結晶層５４の表面を鏡面状にポリッシングし、厚さ３００μmのn型GaN単結晶基板５４を作製する（図４(e)）。

【００７１】このように、図４の作製工程例によれば、$In_rAl_sGa_{(1-r-s)}N$($0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$)単結晶薄膜５２、多結晶$In_tAl_uGa_{(1-t-u)}N$($0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$)基板５３、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶５４の組成がすべて同一であるので、図３の作製方法よりもさらに熱膨張係数差によるクラックの発生や反りが低減され、図３の作製方法よりもさらに高品質の実用的な面積の$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶基板５４が作製される。また構成元素が同一であるので、基板からの不純物も低減される。

【００７２】本発明では、上述したような各作製方法で作製された$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶基板５４を提供できる。そして、$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単結晶５４を成長する工程で、n型やp型ドーパントをドープすることで、所望の伝導型を示す導電性基板を提供できる。

【００７３】すなわち、本発明では、GaN系半導体と熱膨張係数差がほとんどなく、かつ、格子整合性，熱伝導性，へき開性，導電性を備えた大面積の$In_xAl_yGa_{(1-x-y)}N$($0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$)単

結晶基板を提供できる。また、第1の基板50は、サファイア（0001）c面、サファイア（11－20）a面、$MgAl_2O_4$スピネル（111）面、6H－SiC（0001）c面、6H－SiC（1－100）m面等が使用可能であるので、基板の面方向によって、（0001）c面や（1－100）m面を主面とする$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板となる。例えば、第1の基板50にサファイア（0001）c面、サファイア（11－20）a面、$MgAl_2O_4$スピネル（111）面、6H－SiC（0001）c面を使用すれば、（0001）c面を主面とする$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板となり、6H－SiC（1－100）m面基板を使用すれば、（1－100）m面を主面とする$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板となる。

【0074】また、本発明では、上述したように作製された$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板54上に、少なくとも1つのP－N接合を含む一般式$In_vAl_wGa_{(1-v-w)}N$（$0\leqq v\leqq 1$，$0\leqq w\leqq 1$，$v+w\leqq 1$）で表わされるGaN系半導体積層構造を積層して、半導体発光素子を提供できる。

【0075】半導体発光素子は、半導体発光素子のp型，n型層に対応した電極に電流が印加され、P－N接合に電流が注入され、キャリアの再結合によって、発光するものである。半導体発光素子を構成するGaN系化合物半導体積層構造は、少なくとも1つのP－N接合を有し、このP－N接合に電流が注入され、キャリアの再結合によって、発光する構造であれば、ホモ接合、シングルヘテロ接合、ダブルヘテロ接合、量子井戸構造、多重量子井戸構造、その他どのような構造であっても差し支えない。

【0076】また、本発明では、半導体発光素子の基板に$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板54が用いられており、基板がへき開可能であるので、半導体発光素子を半導体レーザとした場合には、平行性，平滑性の良いへき開によるレーザ共振器ミラーを有することができる。さらに、基板を導電性にすることにより（すなわち、$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板54にn型やp型ドーパントをドープすることにより）、基板裏面に電極を形成された発光素子とすることが可能である。

【0077】図5は本発明に係る半導体発光素子の具体例を示す図である。なお、図5の半導体発光素子は半導体レーザとして構成されている。図5を参照すると、この半導体発光素子は、上述したような作製方法で作製した$n-Al_{0.15}Ga_{0.85}N$単結晶基板54上に、n－GaNバッファ層31，$n-Al_{0.15}Ga_{0.85}N$クラッド層32，n－GaN光ガイド層33，$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$多重量子井戸構造活性層34，p－GaN光ガイド層35，$p-Al_{0.15}Ga_{0.85}N$クラッド層36，p－GaNキャップ層37が順次積層された積層構造を有している。

【0078】そして、この積層構造のp型GaNキャップ層37の表面から$p-Al_{0.15}Ga_{0.85}N$クラッド層36の途中までが、幅5μmの残しストライパターンを使用してエッチングされて導波路となるリッジ構造が形成されている。ここで、導波路の方向は、<;1－100>;方向である。

【0079】このようにリッジ構造が形成されることにより露出した$p-Al_{0.15}Ga_{0.85}N$クラッド層36表面には、SiO_2からなる保護層38が堆積されている。また、p－GaNキャップ層37上には、p側オーミック電極39が形成されている。また、$n-Al_{0.15}Ga_{0.85}N$単結晶基板54の裏面には、n側オーミック電極40が形成されている。この半導体レーザの光共振器面は（1－100）m面をへき開することによって形成されている。

【0080】図5の半導体発光素子において、n－GaNバッファ層31，$n-Al_{0.15}Ga_{0.85}N$クラッド層32，n－GaN光ガイド層33，$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$多重量子井戸構造活性層34，p－GaN光ガイド層35，$p-Al_{0.15}Ga_{0.85}N$クラッド層36，p－GaNキャップ層37はMOCVD法によって結晶成長した。

【0081】また、p側オーミック電極39は、Au／Pt／Niを真空蒸着し、700℃の温度で、20分間熱処理して形成した。また、n側オーミック電極40は、Al／Tiを真空蒸着し、熱処理して形成した。

【0082】図5の半導体レーザは、p側オーミック電極39、n側オーミック電極40に電流が印加されると、$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$多重量子井戸構造活性層34に電流が注入され、キャリアの再結合によって発光し、へき開によって形成された共振器面によって、反射増幅が繰り返され、レーザ光として外部に出力される。

【0083】図5の半導体レーザでは、基板54に、クラッド層と同一組成の$n-Al_{0.15}Ga_{0.85}N$単結晶基板を使用しているので、サファイアやGaN基板を使用する場合に比べ、クラッド層のAlの混晶比を大きくしても結晶成長時にクラックが入りにくく、従って、光の閉じ込めに十分な組成と厚さを備えたクラッド層が形成できる。その結果、クラッド層からの光の漏れによるビーム形状の悪化がなく、かつ発振しきい電流密度が低い半導体レーザが作製される。

【0084】図6は本発明に係る半導体基板の他の作製工程例を示す図である。図6の作製工程例では、

a．第1の基板（単結晶基板）10にIn_tAl_uGa

$_{(1-t-u)}$N(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２を形成する工程（図６（ａ））と、
ｂ．第１の基板(単結晶基板)１０から$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２を分離する工程（図６（ｂ））と、
ｃ．$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２を低融点金属１６を介して第２の基板１５に貼り付ける工程（図６（ｃ））と、
ｄ．第２の基板１５に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２上に、低融点金属１６の融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶１７をエピタキシャル成長する工程（図６（ｄ））と、
ｅ．第２の基板１５から$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶１７を低融点金属１６の融点以上の温度で分離する工程（図６（ｅ））とを有し、最終的に、$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶基板１７を作製するようになっている。

【００８５】ここで、第１の基板(単結晶基板)１０としては、サファイア（０００１）ｃ面、サファイア（１１－２０）ａ面、$MaAl_2O_4$スピネル（１１１）面、６Ｈ－ＳｉＣ（０００１）ｃ面、６Ｈ－ＳｉＣ（１－１００）ｍ面等が使用可能である。

【００８６】また、ａの工程において、$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２の結晶成長方法としては、ＭＯＣＶＤ，ＨＶＰＥ，ＭＢＥ等が使用可能であるが、上記方法に限定されるものではなく、第１の基板(単結晶基板)１０に、$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２を結晶成長させることができる方法であれば、その他の方法を用いても良い。また、$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２を成長する前に、ＧａＮやＡｌＮ等の低温バッファ層やその他の層を先に堆積しても差し支えなく、第１の基板(単結晶基板)１０を使用して成長した結晶層の表面層が$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶であれば良い。

【００８７】また、ｂの工程において、第１の基板(単結晶基板)１０から$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２を分離する方法としては、$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２を支持基板に貼り付けた後、化学エッチング，研磨等の方法で第１の基板(単結晶基板)１０を除去する方法や、第１の基板(単結晶基板)１０と$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶層１２との間にエッチング等が可能な層を成長しておいた後にその層をエッチングしリフトオフによって第１の基板(単結晶基板)１０を分離する方法等が使用可能であるが、分離の方法に関しては、上記の方法に特に限定されるものではない。

【００８８】また、ｃの工程において、低融点金属１６としては、その融点が$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)の成長温度と、第２の基板１５を分離する温度よりも低いものであれば、単金属でも合金でも良い。例えば、インジウム、スズ、ガリウム等が使用可能である。また、第２の基板１５としては、後の工程で$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶をエピタキシャル成長する際に、その成長温度、成長雰囲気で安定であれば良く、サファイア，Ｓｉ，石英等を、単結晶，多結晶，非晶質を問わず、使用可能である。

【００８９】また、ｄの工程において、第２の基板１５に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２上に、低融点金属１６の融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶１７をエピタキシャル成長する時、$In_tAl_uGa_{(1-t-u)}N$(0≦t≦1，0≦u≦1，t＋u≦1)単結晶薄膜１２は、溶融金属１６上にあるので、第２の基板１５と$In_xAl_yGa_{(1-x-y)}N$(0≦x≦1，0≦y≦1，x＋y≦1)単結晶１７との熱膨張係数差や結晶構造の違い等の影響を受けずに、単結晶１７の結晶成長が進む。結晶成長の方法は、特に限定するものではないが、厚い単結晶層１７を成長することから、ＨＶＰＥ法や高速のＭＯＣＶＤ法等の成長速度の速い方法が望ましい。また、ｎ型やｐ型ドーパントをドープすることにより、伝導型を制御することが可能である。

【００９０】図７，図８は図６に示した作製工程例の具体例を示す図である。図７，図８の工程例では、半導体基板として、ｎ型ＧａＮ単結晶基板を作製している。

【００９１】図７，図８を参照すると、先ず、直径２インチの（０００１）ｃ面サファイア基板１０上に、ＭＯＣＶＤ法でＧａＮ層１２を成長する。ＧａＮ層１２の成長は、ＭＯＣＶＤ法で行ない、５２０℃で水素ガスをキャリアガスとして、III族原料にトリメチルガリウム、Ｖ族原料にアンモニアを使用して、ＧａＮバッファ層１１を約２５ｎｍ堆積し、その後、１０５０℃に昇温し、ＧａＮ単結晶層１２を１０μｍ成長することによってなされる（図７（ａ））。

【００９２】次いで、有機系の接着剤１３で支持基板１４にＧａＮ単結晶層１２の表面を接着し（図７（ｂ－１））、次いで、サファイア基板１０を研磨装置で研磨除去する（図７（ｂ－２））。

【００９３】次いで、石英基板１５とＧａＮ単結晶層１２とをインジウム１６で接着する（図７（ｃ－１））。

ここで、接着方法としては、石英基板１５上にインジウム１６を載せ、さらにその上に支持基板１４に貼り付けたＧａＮ単結晶層１２をＧａＮ単結晶層１２表面をインジウム１６側にして載せ、インジウム１６の融点以上の温度に加熱し、インジウム１６を溶融状態にして接着する。

【００９４】しかる後、有機溶剤で有機系の接着剤１３を溶解し、支持基板１４を分離する（図８（ｃ－２））。

【００９５】次いで、ＧａＮ単結晶層１２を接着した石英基板１５をＨＶＰＥ装置に移送し、N_2ガスをキャリアガスとして、また、反応ガスにＨＣｌガス、III族原料に金属ガリウム、Ｖ族原料にアンモニアガス、ｎ型ドーパントガスに四塩化珪素（$SiCl_4$）を使用して、１０５０℃でＧａＮ単結晶層１２の表面にｎ型ＧａＮ単結晶１７を３００μｍの厚さに成長する（図８（ｄ））。

【００９６】次いで、ｎ型ＧａＮ単結晶層１７を成長した石英基板１５をインジウム１６の融点以上の温度に加熱し、インジウム１６を溶融状態にして石英基板１５を分離する（図８（ｅ－１））。しかる後、研磨装置を使用して、ＧａＮバッファ層１１を研磨除去し、さらに、ＧａＮ単結晶層１７の表面を鏡面状にポリッシングし、厚さ約３００μｍのｎ型ＧａＮ単結晶基板１７を作製する（図８（ｅ－２））。このようにして、半導体基板として、ｎ型ＧａＮ単結晶基板を作製することができる。

【００９７】図６，図７，図８の作製工程例では、$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶１７の結晶成長後の冷却過程で、低融点金属１６の凝固点までは、$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶層１７は基板１５と結合していないので、$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶層１７を大面積のものにしても、結晶成長温度から低融点金属１６の凝固点までの冷却時における基板１５と$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶層１７との熱収縮差によるクラックの発生や反りが低減される。従って、クラックや反りの低減された大面積の$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板１７を作製することができる。

【００９８】また、第２の基板１５からの$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶層１７の分離を第２の基板１５を損傷することなく容易に行なうことができ、再利用が可能であるので、低コスト化が図られる。さらに、第２の基板１５には、単結晶，多結晶，非晶質等が使用できるので、基板選択の幅が広がり、安価な基板を選択することによって、低コスト化が図られる。

【００９９】なお、上述したｃの工程（図６（ｃ））で、低融点金属１６として室温近傍(約３０℃)に融点をもつＧａ(ガリウム)を使用し、ｄ，ｅの工程（図６（ｄ），（ｅ））における$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶１７のエピタキシャル成長から、第２の基板１５の分離までをＧａを凝固させることなく行なうこともできる。

【０１００】すなわち、この場合には、

ａ．第１の単結晶基板１０に$In_tAl_uGa_{(1-t-u)}N$（$0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$）単結晶薄膜１２を形成する工程（図６（ａ））と、

ｂ．第１の単結晶基板１０から$In_tAl_uGa_{(1-t-u)}N$（$0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$）単結晶薄膜１２を分離する工程（図６（ｂ））と、

ｃ．$In_tAl_uGa_{(1-t-u)}N$（$0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$）単結晶薄膜１２を溶融状態の金属Ｇａ（ガリウム）１６を介して第２の基板１５に貼り付ける工程（図６（ｃ））と、

ｄ．第２の基板１５に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$（$0\leqq t\leqq 1$，$0\leqq u\leqq 1$，$t+u\leqq 1$）単結晶薄膜１２上に、金属Ｇａ（ガリウム）１６の融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶１７をエピタキシャル成長し、金属Ｇａ（ガリウム）１６を凝固させずに冷却させる工程（図６（ｄ））と、

ｅ．第２の基板１５から$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶１７を金属Ｇａ（ガリウム）１６の融点以上の温度で分離する工程（図６（ｅ））とを有し、最終的に、$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶基板１７を作製するようになっている。

【０１０１】このように、ｃの工程（図６（ｃ））で、低融点金属１６として室温近傍(約３０℃)に融点をもつＧａを使用し、ｄ，ｅの工程（図６（ｄ），（ｅ））における$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶１７のエピタキシャル成長から、第２の基板１５の分離までをＧａを凝固させることなく行なうようにすることで、第２の基板１５と$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶１７の熱膨張係数差による結晶成長後の冷却過程での熱歪みの影響を全く受けずに、単結晶基板を作製することが可能となる。

【０１０２】低融点金属１６として室温近傍(約３０℃)に融点をもつＧａを使用し、$In_xAl_yGa_{(1-x-y)}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$x+y\leqq 1$）単結晶１７のエピタキシャル成長から、第２の基板１５の分離までをＧａを凝固させることなく行なう場合の具体例について説明する。なお、この具体例では、半導体基板として、ｎ型ＧａＮ単結晶基板を作製している。

【０１０３】この具体例では、先ず、直径２インチの（０００１）ｃ面サファイア基板１０上に、ＭＯＣＶＤで

ＧａＮ層１２を成長する。ＧａＮ層１２の成長はＭＯＣＶＤで行ない、５２０℃で水素ガスをキャリアガスとして、III族原料にトリメチルガリウム、Ｖ族原料にアンモニアを使用して、ＧａＮバッファ層１１を約２５ｎｍ堆積し、その後、１０５０℃に昇温し、ＧａＮ単結晶層１２を１０μｍ成長することによってなされる（図７（ａ））。

【０１０４】次いで、有機系の接着剤１３で支持基板１４にＧａＮ単結晶層１２の表面を接着し（図７（ｂ－１））、次いで、サファイア基板１０を研磨装置で研磨除去する（図７（ｂ－２））。

【０１０５】次いで、石英基板１５とＧａＮ単結晶層１２とをＧａ(ガリウム)１６で接着する（図７（ｃ－１））。ここで、接着方法としては、石英基板１５上にＧａ(ガリウム)１６を載せ、さらにその上に支持基板１４に貼り付けたＧａＮ単結晶層１２をＧａＮ単結晶層１２表面をＧａ(ガリウム)１６側にして載せ、Ｇａ(ガリウム)１６の融点以上の温度に加熱し、Ｇａ(ガリウム)１６を溶融状態にして接着する。

【０１０６】しかる後、有機溶剤で有機系の接着材１３を溶解し、支持基板１４を分離する（図８（ｃ－２））。このときの温度はＧａ(ガリウム)１６の融点以下とする。

【０１０７】次いで、ＧａＮ単結晶層１２を接着した石英基板１５をＨＶＰＥ装置に移送し、N_2ガスをキャリアガスとして、また、反応ガスにＨＣｌガス、III族原料に金属ガリウム、Ｖ族原料にアンモニアガス、ｎ型ドーパントガスに四塩化珪素（$SiCl_4$）を使用して、１０５０℃でＧａＮ単結晶基板１２の表面にｎ型ＧａＮ単結晶１７を３００μｍの厚さに成長する（図８（ｄ））。

【０１０８】次いで、ｎ型ＧａＮ単結晶１７の成長後、Ｇａ(ガリウム)１６の融点以上の３５℃まで冷却し、この温度を保持して石英基板１５を分離する（図８（ｅ－１））。しかる後、研磨装置を使用して、ＧａＮバッファ層１１を研磨除去し、さらに、ＧａＮ単結晶層１７の表面を鏡面状にポリッシングし、厚さ約３００μｍのｎ型ＧａＮ単結晶基板１７を作製する（図８（ｅ－２））。このようにして、半導体基板として、ｎ型ＧａＮ単結晶基板を作製することができる。

【０１０９】このように、上述のｃの工程（図６（ｃ））で、低融点金属１６として室温近傍(約３０℃)に融点をもつＧａを使用し、ｄ，ｅの工程（図６（ｄ），（ｅ））における$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶１７のエピタキシャル成長から、第２の基板１５の分離までをＧａを凝固させることなく行なうこともできる。この場合には、$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶１７の結晶成長中および成長後の冷却過程においても、金属Ｇａ（ガリウム）１６は溶融状態であるので、$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶層１７は第２の基板１５と結合していない。そのため、$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶層１７は、結晶成長中も成長終了後の冷却時も、第２の基板１５と$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶層１７との熱膨張係数差による熱歪みの影響をまったく受けないので、$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶層１７を大面積にしてもクラックの発生および反りがない。従って、クラックや反りの低減された大面積の$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶基板１７を作製することができる。

【０１１０】また、第２の基板１５は、単結晶，多結晶，非晶質等が使用できるので、基板選択の幅が広がり、安価な基板を選択することができる。さらに、第２の基板１５から$In_xAl_yGa_{(1-x-y)}N$(０≦ｘ≦１，０≦ｙ≦１，ｘ＋ｙ≦１)単結晶層１７を第２の基板１５を損傷することなく、容易に分離することができるので、基板の再利用が可能である。従って、低コスト化が図られる。また、低融点金属に母材元素と同じＧａを使用するので、低融点金属による不純物汚染が低減される。

【０１１１】また、上述した作製工程例において、第１の基板(単結晶基板)１０は、$In_tAl_uGa_{(1-t-u)}N$(０≦ｔ≦１，０≦ｕ≦１，ｔ＋ｕ≦１)単結晶薄膜１２と同程度の熱膨張係数を有しているのが良い。

【０１１２】すなわち、第１の基板(単結晶基板)１０は、その上に結晶成長する$In_tAl_uGa_{(1-t-u)}N$(０≦ｔ≦１，０≦ｕ≦１，ｔ＋ｕ≦１)単結晶薄膜１２と熱膨張係数が同程度であり、$In_tAl_uGa_{(1-t-u)}N$(０≦ｔ≦１，０≦ｕ≦１，ｔ＋ｕ≦１)単結晶薄膜１２が結晶成長するものであれば良い。例えば、ＧａＮの場合には、ＧａＡｓやＧＧＧ（$Gd_3Ga_5O_{12}$）等が使用できる。ＧａＡｓの場合は、（１００）ＧａＡｓを使用することで、立方晶ＧａＮが成長し、（１１１）ＧａＡｓを使用することで、六方晶ＧａＮを成長することができる。

【０１１３】このように、第１の基板(単結晶基板)１０は、$In_tAl_uGa_{(1-t-u)}N$(０≦ｔ≦１，０≦ｕ≦１，ｔ＋ｕ≦１)単結晶薄膜１２と同程度の熱膨張係数を有していることによって、第１の基板１０との熱膨張係数差による$In_tAl_uGa_{(1-t-u)}N$(０≦ｔ≦１，０≦ｕ≦１，ｔ＋ｕ≦１)単結晶薄膜１２の成長後の冷却時に発生する反りやクラックが少なくなる。これにより、大面積基板に比較的厚い$In_tAl_uGa_{(1-t-u)}N$(０≦ｔ≦１，０≦ｕ≦１，ｔ＋ｕ≦１)単結晶層１２を成長することができる。従って、$In_tAl_uGa_{(1-t-u)}N$(０≦ｔ≦１，０≦ｕ≦１，ｔ＋ｕ≦１)単結

晶層１２を第１の基板１０から分離する作業も薄い結晶層を分離する場合に比べて容易になり、歩留まりも向上する。

【０１１４】また、第１の基板１０との熱膨張係数差が小さいので、熱歪みによって、発生する欠陥も熱膨張係数差が大きな基板を使用した場合に比べて低減される。最終的に基板となる$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶層１７は、この欠陥の少ない$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶層１２上に成長するので、欠陥の少ない高品質のものとなる。従って、不純物が少なく、クラックや反りが低減されることに加えて、さらに、大面積で、低コスト、高品質の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板を作製できる。

【０１１５】また、第１の基板（単結晶基板）１０は、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜１２と熱膨張係数が同程度であれば、その上に積層構造を有していても差し支えない。例えば、後述のように、第１の基板１０として、ＧａＡｓ基板上にＡｌＡｓやＧａＡｓを積層していても良い。

【０１１６】また、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜１２の結晶成長方法としては、ＭＯＣＶＤ，ＨＶＰＥ，ＭＢＥ等の手段が使用可能であるが、これは特に限定するものでなく、第１の基板（単結晶基板）１０に、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜１２を結晶成長することができる方法であればその他の方法を用いても良い。

【０１１７】また、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜１２を成長する前に、ＧａＮやＡｌＮ等の低温バッファ層やその他の層を先に堆積しても差し支えなく、第１の基板（単結晶基板）１０を使用して成長した結晶層の表面層が$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶であれば良い。

【０１１８】図９，図１０は図６に示した作製工程例の他の具体例を示す図である。なお、図９，図１０の工程例では、半導体基板として、ｎ型ＧａＮ単結晶基板を作製している。

【０１１９】図９，図１０を参照すると、先ず、直径２インチの（１１１）ＧａＡｓ基板２０上にＭＯＣＶＤ法でＡｌＡｓ層２１，ＧａＡｓ層２２を順次にエピタキシャル成長し、これを第１の基板１０とする。そして、この第１の基板１０上にＧａＮ層１２を成長する。ＧａＮ層１２の成長は、ＭＯＣＶＤ法で行ない、５２０℃で水素ガスをキャリアガスとして、III族原料にトリメチルガリウム、Ｖ族原料にアンモニア、モノメチルヒドラジンを使用して、ＧａＮバッファ層１１を約２５ｎｍ堆積し、その後、７５０℃に昇温し、ＧａＮ単結晶層１１を２０μｍ成長することによってなされる（図９（ａ））。

【０１２０】次いで、有機系の接着剤１３で支持基板１４にＧａＮ単結晶層１２の表面を接着し（図９（ｂ－１））、次いで、フッ酸水溶液に浸し、ＡｌＡｓ層２１を選択的にエッチング除去して、ＧａＡｓ基板２０を分離する（図９（ｂ－２））。

【０１２１】次いで、石英基板１５とＧａＮ単結晶層１２をＧａ（ガリウム）１６で接着する（図９（ｃ－１））。接着方法としては、石英基板１５上にＧａ（ガリウム）１６を載せ、さらにその上に支持基板１４に貼り付けたＧａＮ単結晶層１２をＧａＡｓ層２２をＧａ（ガリウム）１６側にして載せ、Ｇａ（ガリウム）１６の融点以上の温度に加熱し、Ｇａ（ガリウム）１６を溶融状態にして接着する。

【０１２２】しかる後、有機溶剤で有機系の接着材１３を溶解し、支持基板１４を分離する（図１０（ｃ－２））。このときの温度はＧａ（ガリウム）１６の融点以下とする。

【０１２３】次いで、ＧａＮ単結晶層１２を接着した石英基板１５をＨＶＰＥ装置に移送し、N_2ガスをキャリアガスとして、また、反応ガスにＨＣｌガス、III族原料に金属ガリウム、Ｖ族原料にアンモニアガス、ｎ型ドーパントガスに四塩化珪素（$SiCl_4$）を使用して、１０５０℃でＧａＮ単結晶層１２の表面にｎ型ＧａＮ単結晶１７を３００μｍ成長する（図１０（ｄ））。

【０１２４】このように、ｎ型ＧａＮ単結晶１７の成長後、Ｇａ（ガリウム）１６の融点以上の３５℃まで冷却し、この温度を保持して石英基板１５を分離する（図１０（ｅ－１））。しかる後、研磨装置を使用して、ＧａＡｓ層２２、ＧａＮバッファ層１１を研磨除去し、さらに、ＧａＮ単結晶層１７の表面を鏡面状にポリッシングし、厚さ約３００μｍのｎ型ＧａＮ単結晶基板１７を作製する（図１０（ｅ－２））。このようにして、半導体基板として、ｎ型ＧａＮ単結晶基板を作製することができる。

【０１２５】図９，図１０の作製工程例では、第１の基板１０として、（１１１）ＧａＡｓ基板２０にＡｌＡｓ層２１，ＧａＡｓ層２２を順次に積層したものを使用しており、ＡｌＡｓとＧａＡｓとのフッ酸によるエッチングの選択比は非常に大きいので、容易にＡｌＡｓ層２１のみをエッチング除去することが可能である。従って、大面積のＧａＮ単結晶層１２を容易に、しかもＧａＡｓ基板２０を損傷することなく分離することができる。よって、大面積で、低コストのＧａＮ基板を作製することが可能となる。

【０１２６】本発明では、上述したような各作製方法で作製された$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板１７を提供できる。そして、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq$

1，x＋y≦1）単結晶17を成長する工程で、n型やp型ドーパントをドープすることで、所望の伝導型を示す導電性基板を提供できる。

【0127】すなわち、本発明では、GaN系半導体と熱膨張係数差がほとんどなく、かつ、格子整合性，熱伝導性，へき開性，導電性を備えた大面積の$In_xAl_yGa_{(1-x-y)}N$（$0≦x≦1$，$0≦y≦1$，$x+y≦1$）単結晶基板を提供できる。

【0128】また、本発明では、上述したように作製された$In_xAl_yGa_{(1-x-y)}N$（$0≦x≦1$，$0≦y≦1$，$x+y≦1$）単結晶基板17上に、少なくとも1つのP－N接合を含む一般式$In_vAl_wGa_{(1-v-w)}N$（$0≦v≦1$，$0≦w≦1$，$v+w≦1$）で表わされるGaN系半導体積層構造を積層して、半導体発光素子を提供できる。

【0129】半導体発光素子は、半導体発光素子のp型，n型層に対応した電極に電流が印加され、P－N接合に電流が注入され、キャリアの再結合によって、発光するものである。半導体発光素子を構成するGaN系化合物半導体積層構造は、少なくとも1つのP－N接合を有し、このP－N接合に電流が注入され、キャリアの再結合によって、発光する構造であれば、ホモ接合、シングルヘテロ接合、ダブルヘテロ接合、量子井戸構造、多重量子井戸構造、その他どのような構造であっても差し支えない。

【0130】また、本発明では、半導体発光素子の基板に$In_xAl_yGa_{(1-x-y)}N$（$0≦x≦1$，$0≦y≦1$，$x+y≦1$）単結晶基板17が用いられており、基板がへき開可能であるので、半導体発光素子を半導体レーザとした場合には、平行性，平滑性の良いへき開によるレーザ共振器ミラーを有することができる。さらに、基板を導電性にすることにより（すなわち、$In_xAl_yGa_{(1-x-y)}N$（$0≦x≦1$，$0≦y≦1$，$x+y≦1$）単結晶基板17にn型やp型ドーパントをドープすることにより）、基板裏面に電極を形成された発光素子とすることが可能である。

【0131】図11は本発明に係る半導体発光素子の具体例を示す図である。なお、図11の半導体発光素子は半導体レーザとして構成されている。図11を参照すると、この半導体発光素子は、上述したような作製方法で作製したn－GaN単結晶基板17上に、n－GaNバッファ層31，n－$Al_{0.15}Ga_{0.85}N$クラッド層32，n－GaN光ガイド層33，$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$多重量子井戸構造活性層34，p－GaN光ガイド層35，p－$Al_{0.15}Ga_{0.85}N$クラッド層36，p－GaNキャップ層37が順次積層された積層構造を有している。

【0132】そして、この積層構造のp型GaNキャップ層37の表面からp－$Al_{0.15}Ga_{0.85}N$クラッド層36の途中まで、幅5μmの残しストライプパターンを使用してエッチングされて導波路となるリッジ構造が形成されている。ここで、導波路の方向は、〈1－10〉方向である。

【0133】このようにリッジ構造が形成されることにより露出したp－$Al_{0.15}Ga_{0.85}N$クラッド層36表面には、SiO_2からなる保護層38が堆積されている。また、p－GaNキャップ層37上には、p側オーミック電極39が形成されている。また、n－GaN単結晶基板17の裏面には、n側オーミック電極40が形成されている。この半導体レーザの光共振器面は（1－100）面をへき開することによって形成されている。

【0134】図11の半導体発光素子において、n－GaNバッファ層31，n－$Al_{0.15}Ga_{0.85}N$クラッド層32，n－GaN光ガイド層33，$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$多重量子井戸構造活性層34，p－GaN光ガイド層35，p－$Al_{0.15}Ga_{0.85}N$クラッド層36，p－GaNキャップ層37は、MOCVD法によって結晶成長した。

【0135】また、p側オーミック電極39は、Au／Pt／Niを真空蒸着し、700℃の温度で、20分間熱処理して形成した。また、n側オーミック電極40は、Al／Tiを真空蒸着し、熱処理して形成した。

【0136】図11の半導体レーザは、p側オーミック電極39，n側オーミック電極40に電流が印加されると、$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$多重量子井戸構造活性層34に電流が注入され、キャリアの再結合によって発光し、へき開によって形成された共振器面によって、反射増幅が繰り返され、レーザ光として外部に出力される。

【0137】このように、本発明では、上述したように作製された$In_xAl_yGa_{(1-x-y)}N$（$0≦x≦1$，$0≦y≦1$，$x+y≦1$）単結晶基板17上に、少なくとも1つのP－N接合を含む一般式$In_vAl_wGa_{(1-v-w)}N$（$0≦v≦1$，$0≦w≦1$，$v+w≦1$）で表わされるGaN系半導体積層構造を積層して、半導体発光素子が構成されているので、格子不整合や熱膨張係数の違いによる欠陥の発生が抑制された高品質な結晶層からなる発光素子を提供できる。また、基板裏面に電極が形成された発光素子やへき開で形成した共振器ミラーを有する半導体レーザを作製することも可能である。

【0138】

【発明の効果】以上に説明したように、請求項1記載の発明によれば、第1の基板に$In_rAl_sGa_{(1-r-s)}N$（$0≦r≦1$，$0≦s≦1$，$r+s≦1$）単結晶薄膜を形成する工程と、$In_rAl_sGa_{(1-r-s)}N$（$0≦r≦1$，$0≦s≦1$，$r+s≦1$）単結晶薄膜を$In_xAl_yGa_{(1-x-y)}N$（$0≦x≦1$，$0≦y≦1$，$x+y≦1$）単結晶と熱膨張係数がほぼ同等である第2の基板に貼り付ける工程と、第1の基板から$In_rAl_sGa_{(1-r-s)}N$（$0≦r≦1$，$0≦s≦1$，$r+s≦1$）単結晶薄膜を分離

する工程と、第２の基板に貼り付けられた$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜上に、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶をエピタキシャル成長する工程と、第２の基板から$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を半導体基板として作製するので、熱膨張係数差の大きな基板に厚く成長することによるクラックの発生や反りがなく、実用的な面積の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板が作製できる。また、第２の基板は、熱膨張係数が$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶とほぼ同等であるので、その結晶構造や格子定数は異なっても差し支えなく、これにより、基板選択の幅が増え、安価な基板を選択することで、低コストで$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板が作製できる。

【０１３９】また、請求項２記載の発明によれば、請求項１記載の半導体基板の作製方法において、第２の基板は、多結晶$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）基板であるので、熱膨張係数差の大きな基板に厚く成長することによるクラックの発生や反りがなく、実用的な面積の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板が作製できる。また、構成元素が同一であるので、基板からの不純物の混入が低減できる。

【０１４０】また、請求項３記載の発明によれば、請求項２記載の半導体基板の作製方法において、$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜、多結晶$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）基板、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶の組成がすべて同一であるので、熱膨張係数差によるクラックの発生や反りがより一層低減され、より高品質の実用的な面積の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板が作製できる。また構成元素が同一であるので、基板からの不純物も低減される。

【０１４１】請求項４記載の発明によれば、第１の基板に$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を形成する工程と、第１の基板から$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を分離する工程と、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を低融点金属を介して第２の基板に貼り付ける工程と、第２の基板に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜上に、低融点金属の融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶をエピタキシャル成長する工程と、第２の基板から$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を低融点金属の融点以上の温度で分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を半導体基板として作製するので、クラックや反りが低減された実用的な面積の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板を低コストで作製することができる。

【０１４２】また、請求項５記載の発明によれば、第１の基板に$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を形成する工程と、第１の基板から$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を分離する工程と、$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜を溶融状態の金属Ｇａを介して第２の基板に貼り付ける工程と、第２の基板に貼り付けられた$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜上に、金属Ｇａの融点以上の温度で、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶をエピタキシャル成長し、金属Ｇａを凝固させずに冷却させる工程と、第２の基板から$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を金属Ｇａの融点以上の温度で分離する工程とにより、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶を半導体基板として作製するので、不純物が少なく、クラックや反りが低減された実用的な面積の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板を低コストで作製することができる。

【０１４３】また、請求項６記載の発明によれば、請求項４または請求項５記載の半導体基板の作製方法において、前記第１の基板は$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜と同程度の熱膨張係数を有しているので、クラックや反りが低減された実用的な面積の高品質な$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板を低コストで作製することができる。

【０１４４】また、請求項７記載の発明によれば、請求項１乃至請求項６のいずれか一項に記載の作製方法によって作製された$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶からなるので、ＧａＮ系半導体との格子整合性，熱伝導性，へき開性，導電性を備えた大面積の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板を提供できる。

【０１４５】また、請求項８記載の発明によれば、請求項７の$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶の半導体基板上に、少なくとも

一つのP-N接合を含む一般式$In_vAl_wGa_{(1-v-w)}N$（$0 \leqq v \leqq 1$，$0 \leqq w \leqq 1$，$v+w \leqq 1$）で表わされるGaN系半導体積層構造が積層されて構成されているので、欠陥が低減された高品質な結晶層からなる半導体発光素子を提供できる。また、基板裏面に電極が形成され、へき開による共振器ミラーを有する半導体レーザを提供できる。

【図面の簡単な説明】

【図１】本発明に係る半導体基板の作製工程例を示す図である。

【図２】図１に示した半導体基板の作製工程例の具体例を示す図である。

【図３】第２の基板を多結晶$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）基板にする場合の作製工程例を示す図である。

【図４】$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜、多結晶$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）基板、$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶の組成をすべて同一にする場合の作製工程例を示す図である。

【図５】本発明に係る半導体発光素子の具体例を示す図である。

【図６】本発明に係る半導体基板の作製工程例を示す図である。

【図７】図６に示した半導体基板の作製工程例の具体例を示す図である。

【図８】図６に示した半導体基板の作製工程例の具体例を示す図である。

【図９】図６に示した半導体基板の作製工程例の具体例を示す図である。

【図１０】図６に示した半導体基板の作製工程例の具体例を示す図である。

【図１１】本発明に係る半導体発光素子の具体例を示す図である。

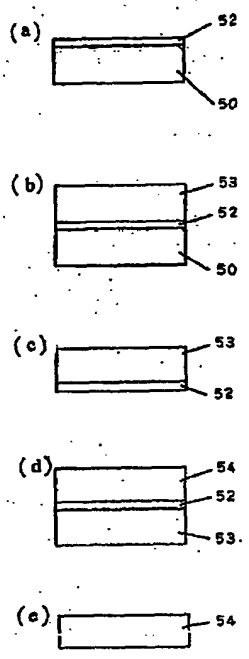
【図１２】従来の半導体レーザを示す図である。

【図１３】従来の半導体レーザを示す図である。

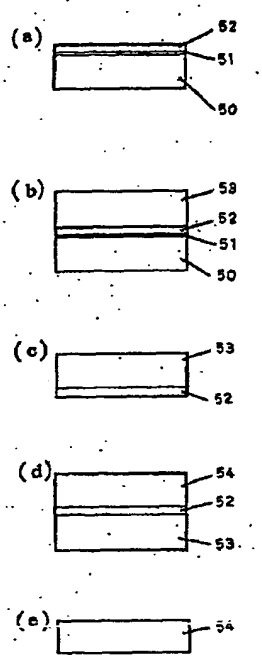
【符号の説明】

１０	第１の基板(単結晶基板)
１１	ＧａＮバッファ層
１２	$In_tAl_uGa_{(1-t-u)}N$（$0 \leqq t \leqq 1$，$0 \leqq u \leqq 1$，$t+u \leqq 1$）単結晶薄膜
１３	有機系の接着剤
１４	支持基板
１５	第２の基板
１６	低融点金属（インジウムまたはガリウム）
１７	$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶基板
２０	(１１１)ＧａＡｓ基板
２１	ＡｌＡｓ層
２２	ＧａＡｓ層
３１	ｎ－ＧａＮバッファ層
３２	ｎ－$Al_{0.15}Ga_{0.85}N$クラッド層
３３	ｎ－ＧａＮ光ガイド層
３４	$In_{0.15}Ga_{0.85}N$／$In_{0.02}Ga_{0.98}N$多重量子井戸構造活性層
３５	ｐ－ＧａＮ光ガイド層
３６	ｐ－$Al_{0.15}Ga_{0.85}N$クラッド層
３７	ｐ－ＧａＮキャップ層
３８	SiO_2からなる保護層
３９	ｐ側オーミック電極
４０	ｎ側オーミック電極
５０	第１の基板（単結晶基板）
５１	ＧａＮバッファ層
５２	$In_rAl_sGa_{(1-r-s)}N$（$0 \leqq r \leqq 1$，$0 \leqq s \leqq 1$，$r+s \leqq 1$）単結晶薄膜
５３	第２の基板
５４	$In_xAl_yGa_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$x+y \leqq 1$）単結晶
１１１	(０００１)サファイア基板
１１２	ｎ型ＧａＮ低温バッファ層
１１３，１３２	ｎ型のＧａＮからなる高温バッファ層
１１４	SiO_2選択成長マスク
１１５，１３３	ｎ－$In_{0.1}Ga_{0.9}N$クラック防止層
１１６，１３４	ｎ－$Al_{0.14}Ga_{0.86}N$／ＧａＮ ＭＤ－ＳＬＳ(モジュレーションドープ歪み超格子)クラッド層
１１７，１３５	ｎ－ＧａＮ光ガイド層
１１８，１３６	$In_{0.15}Ga_{0.86}N$／$In_{0.02}Ga_{0.98}N$ ＭＱＷ活性層
１２０，１３８	ｐ－ＧａＮ層光ガイド層
１２１，１３９	ｐ－$Al_{0.14}Ga_{0.86}N$／ＧａＮ ＭＤ－ＳＬＳクラッド層
１２２，１４０	ｐ型ＧａＮ層キャップ層
１２３，１４３	Ｐ側電極
１２４，１４２	SiO_2保護層
１２５，１４１	ｎ側電極
１３１	（０００１）面ＧａＮ基板

【図1】



【図2】



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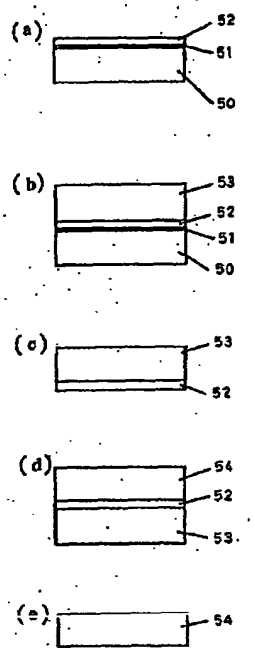
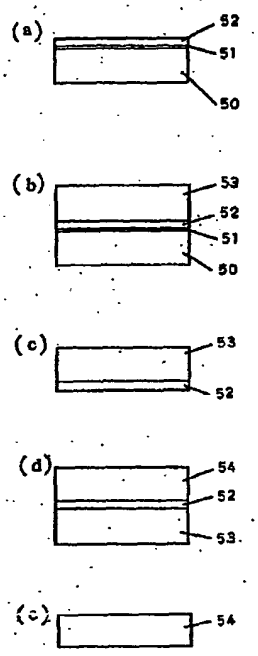


【図4】



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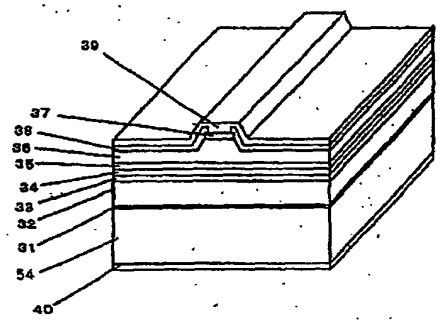

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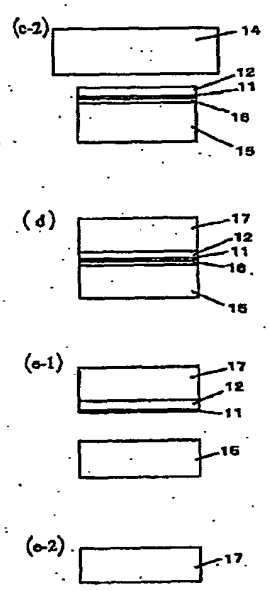

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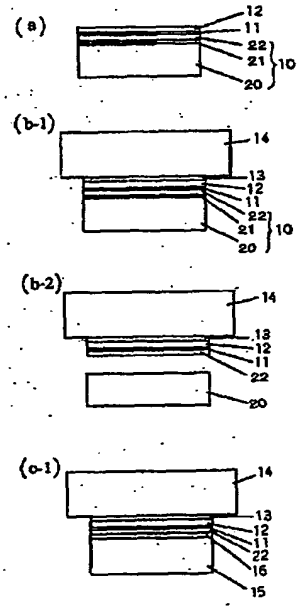

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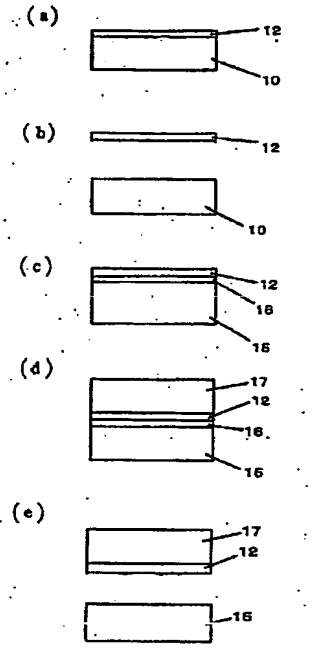

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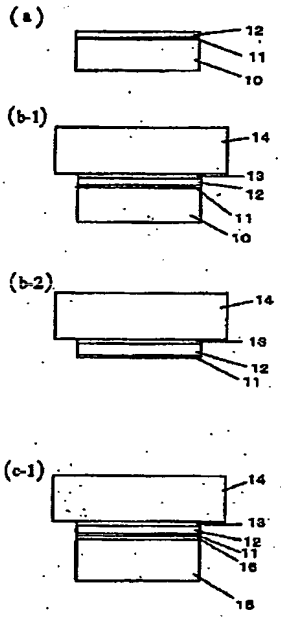

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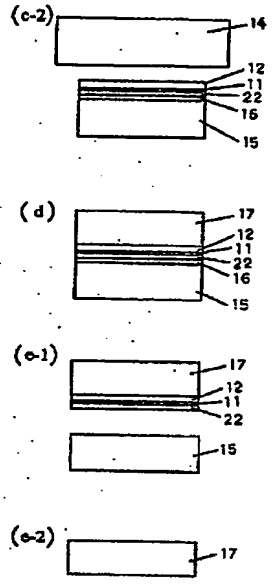

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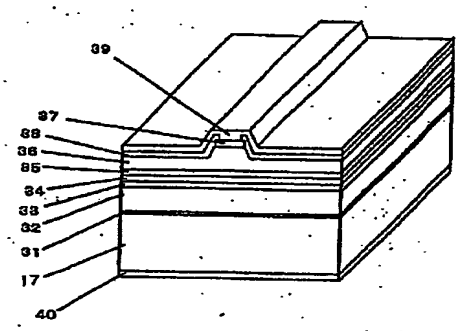

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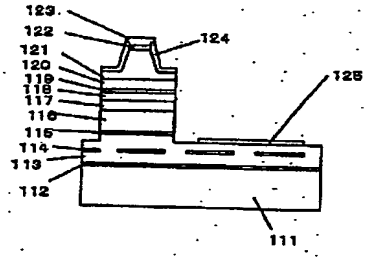

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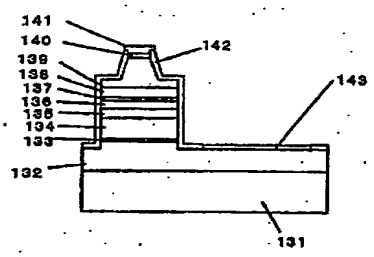

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DA53 DA54 DA55 DA57 DA62
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HA11 HA12 HA14 HA16
5F073 AA13 AA74 CA07 CB02 CB04
CB05 CB07 DA05 EA29
5F103 AA04 DD01 GG01 HH03 HH04
JJ01 JJ03 KK01 LL01 LL02
LL03 LL16 LL17 LL18 PP03
PP07 RR08 RR10